Novel Concept of Reducing OVR at the Output of SEPIC Converter using Programmable Capacitors

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Abstract: In this paper, a novel methodology is proposed to reduce output voltage ripple (OVR) of the single-ended primary-inductor-converter (SEPIC). The mathematical analysis of the SEPIC converter is performed to compute suitable values of capacitance and switching frequency for optimal reduction in the OVR. The OVR in SEPIC converter is analyzed in the presence of two- dimensional effect: first by varying the values of the programmable capacitor using digital controller; second by changing the switching frequency of the switching signal. The comprehensive mathematical analysis of the OVR in SEPIC is performed for three modes. The obtained results of proposed methodology for the reduction of the OVR in SEPIC converter are verified through MATLAB simulation.

Keywords: SEPIC Converter; Output voltage ripple; Digital capacitor; Switching frequency.

Table 1. List of Symbols

Description	Symbols
Input Voltage	Yi
Output Voltage	Yo
Variable Capacitor	ΔC_2
Output Voltage Ripple (OVR)	μ
Change in OVR	ν
Change in OVR	ñ
switching frequency	F
Time	T
Duty cycle	D
Critical Inductor	X
Equivalent Critical Inductor	Ξ
Load Current	i_{Load}
Equivalent Inductance	L_{eq}

1. Introduction

Today, converters are extensively used in electrical devices and systems such as aeronautical applications [1], DC power supply [2], [3], fuel cell [4], automobiles [5], electrical vehicles [6], [7], control of power factor [8] and DC power lightening system [9]. There are different types of converters which include buck converter, boost converter, buck-boost converter, Cuk converter, Zeta converter and etc. The continuous research efforts have resulted in the expanse of the power electronics'. Many researchers have made extensive efforts to examine the output behavior of converters by small modifications in their circuits. Since the main components of the PWM converter circuit include inductors and capacitors and it is a well-established fact that there is no

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power loss when power exchange between a pure inductor and a pure capacitor takes place. The PWM switching signals can be used to control the transfer of power from input to output when the resonant switching frequency is lower than the switching frequency of the inductor-capacitor network [10]. The most popular PWM converter is buck converter and all other converters are developed based on the same approach that is used for buck converters [11]. These include boost converter [11], [12], buck-boost converter [11], [13], SEPIC converter [12], [14], Zeta converter [14], [15], flyback [16] and Cuk converter [17]. Many other PWM converters are produced by putting the dc transformers in buck-boost converter, for example, full-bridge, half-bridge, push-pull and etc [18]. The advancement in PWM converters has been crossing over a century for now; in addition, many other converters have been manufactured, for example, quasi-resonant [19], Zsource [20] and switched-inductor hybrid converters [21], and these converters are performing optimally in several appliances successfully. Many researchers proposed an idea to produce PWM converters by using switching cell method. Switching in capacitor and inductor makes it possible to produce dc/dc converter, which is helpful to obtain a huge step-up or step-down conversion [22]. The output of the DC/DC power converter is the regulated voltage because the output of the power converters is controlled and regulated by switching techniques [23]. This, subsequently, results in ripple in the output voltage of these power converters. This unwanted output voltage ripple (OVR) decreases the working efficiency of power converters [24]. Many researchers have rendered some methodologies to minimize the OVR in the converter's output. A complicated control approach in [25] is developed using a PID controller with a resonant controller paralleled to minimize the OVR. A new remodeled buck-boost converter by allegory has been introduced which has continuous output current and low current stress for components but it has a limited range of voltage conversion [26]. Buck-boost converter with an extra LC filter has been introduced to reduce the OVR but it is expensive and complicated [27]. Being complex this method can only be used for low voltages and high current. In addition, high electromagnetic interference is produced by using more elements such as capacitors and inductors [28]. The authors have proposed a new idea of SEPIC converter for OVR minimization in continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

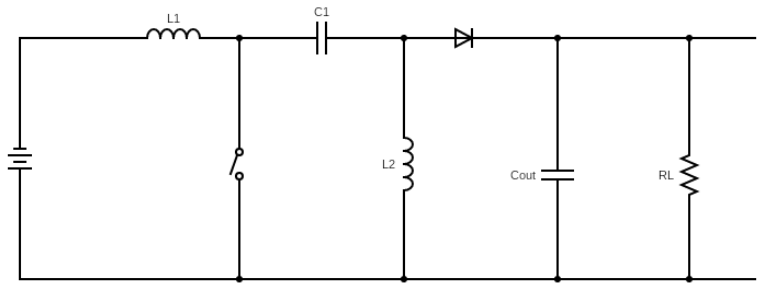


Figure 1. Circuit Diagram of SEPIC Converter

Figure 1 presents the circuit diagram of the SEPIC converter, which comprises of FET working as a switch and two inductors of suitable values along with the output capacitor [29][30]. The input side of the SEPIC converter is energized form a renewable DC energy source with an input voltage y_{in} and output voltage y_{out} is available at the output side. The working of a SEPIC converter is similar to any other conventional buck-boost converter with the difference that polarity of the output voltage is the same as the input voltage whereas in buck-boost converter the output polarity is opposite to the input polarity [31]. The ripple current and voltages are considerably high at the output [32]. In [33] tried to reduce OVR in converters by using critical inductor in both continuous conduction mode and discontinuous conduction mode.

In this article, a new methodology is introduced which uses a programmable capacitor [34] and alteration in switching frequency. The schematic of programmable capacitor circuit is presented in Figure 2.

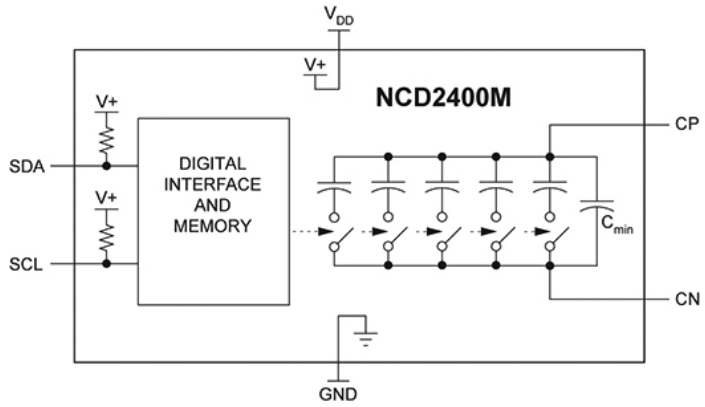


Figure 2. Schematics of programmable capacitor [32]

This article has three main sections: Section 2, describes the flow of energy in CCM mode and DCM mode and also gives the information about load current and inductors' current. Section 3, describes evaluation of the equivalent critical inductance in operational modes because this acts as a main boundary between CCM and DCM. Also, OVR minimization methodology is elaborated in detail. In section 4, the results of CISM-CCM, IISM-CCM and IISM-DCM in both buck and boost mode of a SEPIC converter are presented.

2. Energy Transfer in Modes of Sepic

The working operation of the SEPIC converter consists of two modes, continuous conduction mode (CCM) and discontinuous conduction mode (DCM) as shown in Figure 3. The Boundary between these two modes is a specific value of inductor. This called as the equivalent critical inductor (ξ) [35]. The (CCM) and (DCM) are further divided into complete induction supply mode (CISM), Incomplete induction supply mode (IISM) respectively. In Continuous Conduction Mode (CCM) the value of current in both inductors is positive and remains the same during the whole time. In CISM load current i_{Load} is less than the sum of currents in both inductors L_1 and L_2, whereas in IISM mode the total current of both inductors is lower than the load current i_{Load}. *Complete Induction Supply Mode:* The sum of both inductors currents is higher than the load current $_{Load}$. During the time interval t_{on} the voltages of both inductors are considered as y_{in} and y_{C1}remains constant, while the current of both inductors $i_{L1}$and i_{L2}rises gradually from least possible value to maximal value. At the same time, capacitor current $i_{C1}$is the same as inductor current i_{L2}but has negative value. Capacitor current i_{C1}decreases gradually, while the voltages of capacitor C_2becomesy_{out}, with the diode being reverse biased. The current i_{Load} is given by capacitor C_2. Suppose that for a large value of capacitor C_2 the load current i_{Load} is stable and y_{out} is diminished from high value to low value. At time interval t_{off}, the output voltage is negative chronologically, while the current of both inductors is fallen from(i_{LP1}&i_{LP2})to(i_{Ly1}&i_{Ly2}) gradually. When inductor $L_1$is discharged the capacitor is charged, therefore, it can be said that current of capacitor C_1 is equal to the inductor L_1 current. On the other hand, capacitor current $_{C2}$ is equal to the sum of currents of both inductors (i_{L1}+i_{L2}). If any change occurs in inductors currents (i_{L1}&i_{L2}), the capacitor current also changes while at the same time, i_{Load} is less than the sum of i_{L1} and i_{L2}. The Voltage across the output is changed from lower value to higher value. The sequence of power flow in *incomplete inductor supply mode* as well as in the discontinuous conduction mode is similar to *complete induction supply mode*. Moreover, this sequence of operation in SEPIC converter is discussed in detail in [36].

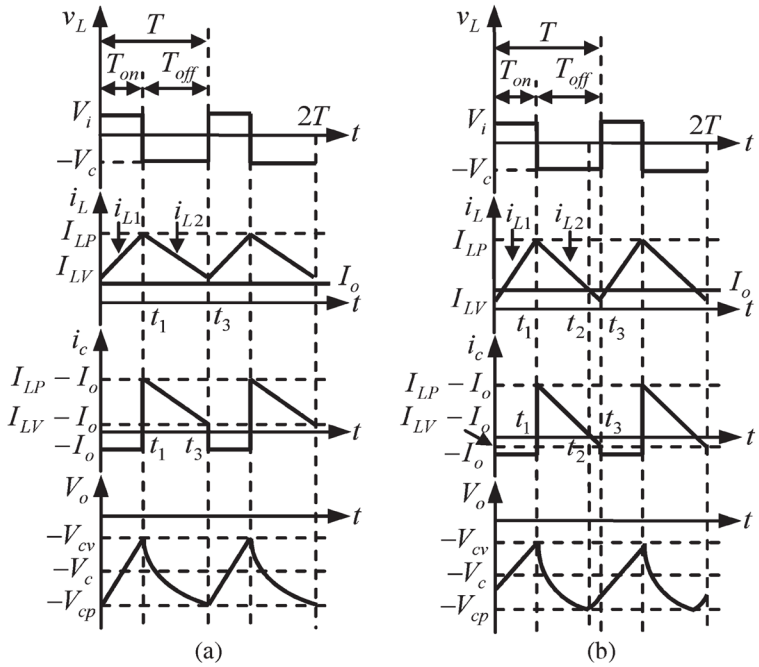


Figure 3. Inductor voltage, inductor current, capacitor current, and output voltage waveforms of buck boost converter (a)CISM-CCM. (b)IISM-CCM.[33]

3. Calculation of Equivalent Critical Inductor in Operational Modes

From above discussion it can be inferred that there are two operational modes in SEPIC converter i.e. CCM and DCM, and these two modes can be differentiated by the equivalent critical inductor (ξ). Also, in CCM mode there are further two modes i.e. CISM and IISM. These two modes are separated by a critical value of the inductor (χ). The equivalent inductance L_{eq} is equal to parallel combination of L_1 and L_2, but in IISM-CCM, the value of equivalent inductance L_{eq} can be varied between the equivalent lower value of critical inductor i.e. (ξ) and upper value of the critical inductor i.e. (χ). In DCM there is only IISM. In IISM-DCM the equivalent inductance L_{eq} is less than the critical inductance (χ). For the sake of mathematical analysis we start with the following equations which are mentioned in [37].

$$\frac{R_L(1-d)^2}{2f} = \xi \tag{1}$$

$$\frac{R_L(1-d)^2}{2fd} = \chi \tag{2}$$

$$\frac{t_{on}}{t_{on}+t_{off}} = d \tag{3}$$

The value of duty cycle$d$ ranges between 0 and 1. The upper value of critical inductance (χ) can be given by Eq. (2) and the lower value of critical inductance (ξ) can be obtained by Eq. (1). These equations are used for the case when SEPIC converter work in Continuous Conduction Mode (CCM). The duty cycle can be given by

$$\frac{yo}{(yo+yi)} = d \tag{4}$$

So the value of the equivalent critical inductance (ξ) and the critical inductance (χ) can be expressed in the following equations by using the value of d in Eqs. (1), (2).

$$\frac{R_L(yi)^2}{2f(yi+yo)^2} = \xi \tag{5}$$

$$\frac{R_L(yi)^2}{2f(yo)(yi+yo)^2} = \chi \tag{6}$$

Calculation of output voltage ripple in CISM-CCM

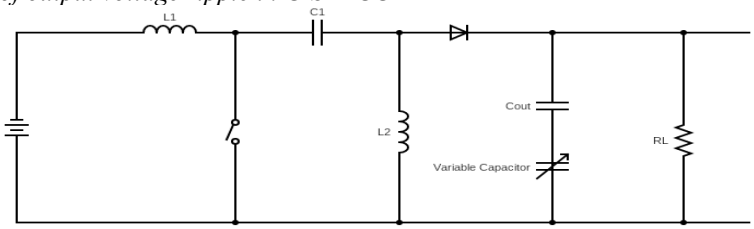


Figure 4. Proposed Methodology for SEPIC converter

The voltage ripple across the capacitor i.e.μ can be written as

$$\frac{-1}{C_2}\int_0^{t_{on}} iC_2(x)dx = \mu \tag{7}$$

At time interval (t_{on}), the value of (i_C2) is following.

$$i_{C_2}(t_{on}) = -i_{Load} \tag{8}$$

Eq. (9) can be achieved by the utilitarian of Eqs.(3)and(8) in Eq.(7).

$$\frac{ti_{Load}d}{C_2} = \mu \tag{9}$$

Eq.(9) can further bare formed intoEq.(10), by using the values of time period t and load current, so get the following formula while t=$\frac{1}{f}$ and $i_{Load} = \frac{yo}{R_L}$.

$$\frac{yo^2}{R_L f(C_2)(yi+yo)} = \mu \tag{10}$$

μ represents the output voltage ripple. Now we proceed further towards the crucial part of the proposed research which is the effect of variation of capacitor on the output voltage ripple. For analysing the effect of change in capacitor value on OVR, rewrite the Eq (7) by replacing the C_2 with ($C_2 + \Delta C_2$).

$$\frac{-1}{\Delta C_2 + C_2}\int_0^{t_{on}} iC_2(x)dx = \nu \tag{11}$$

By simplifying Eq. (11).

$$\frac{ti_{Load}d}{C_2 + \Delta C_2} = \nu \tag{12}$$

Put the value of i_{Load}, time period and duty cycle in above Eq. (12) to get the following equation.

$$\frac{yo^2}{R_L f(C_2+\Delta C_2)(yi+yo)} = \nu \tag{13}$$

Eq. (13) illustrates the output ripple voltages by using a variable capacitor. The change in OVR can be written as

$$\nu - \mu = \tilde{n} \tag{14}$$

Put the value of μ and v from (10) and (13) respectively in Eq. (14).

$$\frac{yo^2}{R_L f(C_2+\Delta C_2)(yi+yo)} - \frac{yo^2}{R_L f C_2(yi+yo)} = \tilde{n} \tag{15}$$

$$-\frac{\Delta C_2 yo^2}{C_2^2 + C_2 \Delta C_2 R_L f(yi+yo)} = \tilde{n} \tag{16}$$

The above equation elaborates the fact that the value of change in OVR i.e.ϱ is dependent on the valueof capacitor and switching frequency. So, by using the digital capacitor or programmable capacitor, wecan control the output voltage ripple. Similarly, a suitable value of switching switching frequency canhelp in decreasing the OVR.

B. Calculation of Output Voltage ripple in IISM-CCM

By taking integration of capacitor current i_{C2} and can get value of OVR at time duration from t_1 to t_2

$$\frac{1}{C_2}\int_{t_1}^{t_2} iC_2(x)dx = \mu \tag{17}$$

Eq. (18) elaborates the value of the capacitor current i_{C2}. When time is off [34].

$$i_{L1} + i_{L2} - i_{Load} = i_{C2} \tag{18}$$

Eq. (19) shows the value of the 1st inductor current.

$$i_{LP1} + \frac{yi - yo - y_{C1}}{L_1} = i_{L1} \tag{19}$$

Eq. (20) explains the value of the second inductor current.

$$i_{LP2} - \frac{yo}{L_2} = i_{L2} \tag{20}$$

Eqs. (19) and (20) is achieved when $t_1 = 0$ and the voltage of C_1 is following.

$$y_{C1} = yi \tag{21}$$

Eq. (22) shows the value of t_2

$$(i_{LP1} + i_{LP2} - i_{Load}) - \frac{Leq}{yo} = t_2 \tag{22}$$

Resolving Eqs. (18), (22) when $t_1 = 0$ and figure out new Eq. (23).

$$(i_{LP1} + i_{LP2} - i_{Load})^2 \frac{Leq}{2yoC_2} = \mu \tag{23}$$

Current of both inductors are:

$$i_{Load}[\frac{1}{1-d}+\frac{R_L}{2Leqf}(1-d)]=i_{LP1}+i_{LP2} \tag{24}$$

Apply Eqs. (4) and (24) in Eq. (23) then find a new Eq. (25).

$$(\frac{yi}{2Leqf(yi+yo)}+\frac{yo}{R_L yi})^2\frac{Leqyo}{2C_2}=\mu \tag{25}$$

If use a variable capacitor in IISM - CCM. New Eq. (26) is achieved.

$$\frac{-1}{\Delta C_2+C_2}\int_{t1}^{t2} iC_2(x)dx=\nu \tag{26}$$

Eq. (27) tells the value of the second current.

$$i_{L1}+i_{L2}-i_{Load}=i_{C2} \tag{27}$$

Put all the above Eqs. and do same process which performed in above section, then get the followingequation.

$$(\frac{yi}{2Leqf(yi+yo)}+\frac{yo}{R_L yi})^2\frac{Leqyo}{2(C_2+\Delta C_2)}=\nu \tag{28}$$

Put Eqs. (25) and (28) in Eq. (29)

$$\nu-\mu=\tilde{n} \tag{29}$$

$$(\frac{yi}{2Leqf(yi+yo)}+\frac{yo}{R_L yi})^2\frac{Leqyo}{2(C_2+\Delta C_2)}=\varrho \tag{30}$$

$$(\frac{yi}{2Leqf(yi+yo)}+\frac{yo}{R_L yi})^2\frac{Leqyo}{2C_2}-\frac{\Delta C_2 Leqyo}{2((C_2)^2+C_2\Delta C_2)}(\frac{yi}{2Leqf(yi+yo)}+\frac{yo}{R_L yi})^2=\tilde{n} \tag{31}$$

Eq. (31) define that change in OVR in IISM-CCM is depended upon capacitor value, switching frequency and input-output voltages.

C. Calculation of Output Voltage ripple in IISM-DCM

During the time duration from t_1 to t_2 as shown in Fig. 3 , the value of OVR can be achieved.

$$\frac{1}{C_2}\int_{t_1}^{t_2} iC_2(x)dx=\mu \tag{32}$$

$$(i_{LP1}+i_{LP2}-i_{Load})^2\frac{Leq}{2C_2 yo}=\mu \tag{33}$$

Eq. (34) describes the value of the first inductor.

$$i_b+\frac{yi}{L_1}dt=i_{LP1} \tag{34}$$

Eq. (35) is expressing the value of the second inductor.

$$\frac{yi}{L_1}dt - i_b = i_{LP2} \tag{35}$$

Applying Eq.s (34), (35) in Eq. (33) and $t = \frac{1}{f}$

$$\frac{Leq}{2C_2 yo}\left(\frac{dyi}{Leqf} - i_{Load}\right)^2 = \mu \tag{36}$$

Eq. (37) presents the duty cycle value when converter works in DCM.

$$\frac{yo}{yi}\sqrt{\frac{2Leqf}{R_L}} = d \tag{37}$$

Apply Eq. (37) in Eq. (36) and put $iLoad = \frac{yo}{R_L}$. So get a new value of OVR.

$$\frac{Leqyo}{2C_2}\left(\sqrt{\frac{2}{fLeqR_L}} - \frac{1}{R_L}\right)^2 = \mu \tag{38}$$

If we use a variable capacitor in IISM-DCM.

$$\frac{-1}{\Delta C_2 + C_2}\int_{t1}^{t2} iC_2(x)dx = \nu \tag{39}$$

$$\frac{Leqyo}{2(C_2 + \Delta C_2)}\left(\sqrt{\frac{2}{fLeqR_L}} - \frac{1}{R_L}\right)^2 = \nu \tag{40}$$

If subtract Eq. (38) from Eq. (40) then achieve a new equation.

$$\nu - \mu = \tilde{\text{n}} \tag{41}$$

$$\frac{Leqyo}{2(C_2 + \Delta C_2)}\left(\sqrt{\frac{2}{fR_L Leq}} - \frac{1}{R_L}\right)^2$$

$$-\frac{Leqyo}{2C_2}\left(\sqrt{\frac{2}{fR_L Leq}} - \frac{1}{R_L}\right)^2 = \tilde{\text{n}} \tag{42}$$

By the simplification of Eq. (42) and gain Eq. (43), which is describing the value of the change in voltageripple by changing the value of capacitor.

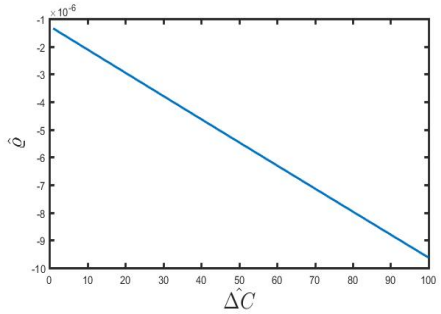
$$-\frac{Leqyo\Delta C_2}{2(C_2^2 + C_2\Delta C_2)}\left(\sqrt{\left(\frac{2}{fR_L Leq}\right)} - \frac{1}{R_L}\right)^2 = \tilde{\text{n}} \tag{43}$$

4. Results and Discussion

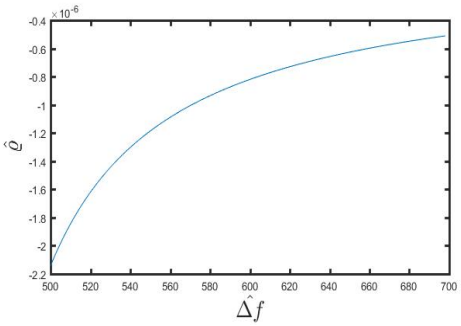
To verify the proposed methodology decreasing the output voltage ripple in the SEPIC converter, MATLAB simulation environment is used. The results of different modes of proposed methodologies of reducing OVR are presented in the following paragraphs. There are two major modes of SEPIC Converter: continuous conduction mode (CCM) and discontinuous conduction mode (DCM), the CCM is divided into two categories; Complete Induction Supply Mode (CISM) and Incomplete Induction Supply Mode (IISM)whereas DCM has only Incomplete Induction Supply Mode (IISM). Each mode has three simulation results. The circuit element value soft proposed converter in buck mode are input voltage y_i is80V, output voltage y_o is 60 V, capacitor $C_2$is 28.5 mF, resistor is 50 ohm, switching frequency is 15 kHz with the change of 500Hz, variable capacitor ΔC_2 is 0.03mF. In boost mode values are: input voltagey_i is 120 V, output voltage y_o is 150 V, capacitor $C_2$is 43 mF, resistor is 250 ohm, switching frequency is

15kHz with the change of 500Hz, variable capacitor ΔC_2 is 0.03mF and value of equivalent inductance L_{eq} is 0.4mH.

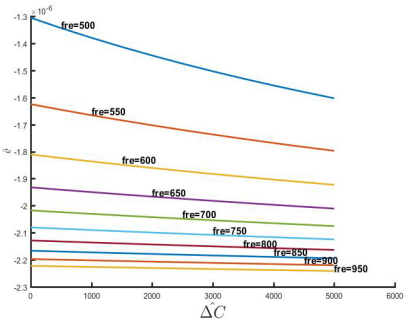
A. CISM-CCM



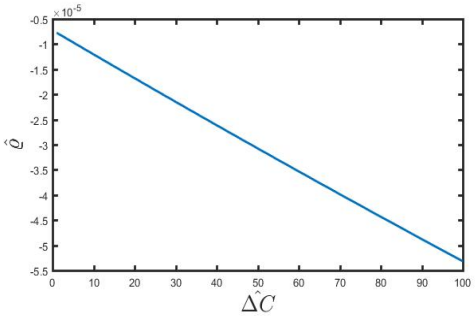
(a) Graph of Variable Capacitor



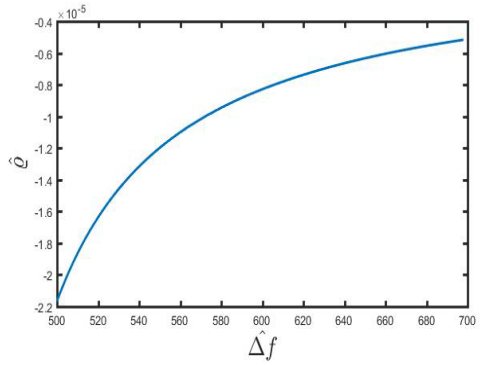
(b) Graph of Variable switching frequency (c)



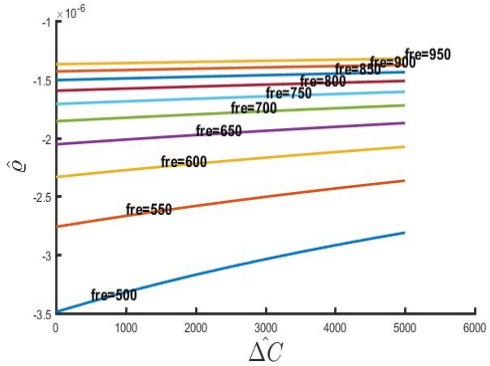
c. Graph of Variable Capacitor and switching frequency



(d) Graph of Variable Capacitor



(e) Graph of Variable switching frequency



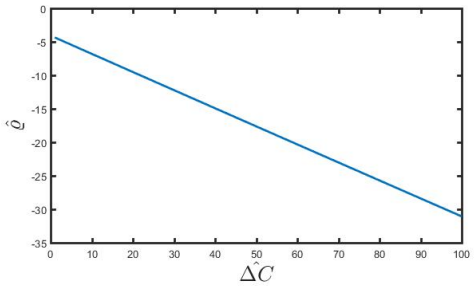
(f) Graph of Variable Capacitor and switching frequency

Figure 5. change in output voltage ripple (ϱ) of buck and boost modes in IISM-CCM of SEPIC converter. (a) reports the result of a variable capacitor, (b) defines the result of a variable switching frequency and(c) represents the result of variable capacitor and switching frequency in buck mode while (d) states the result of a variable capacitor, (e) narrates the result of variable switching frequency and (f) defines the result of a variable capacitor and switching frequency in boost mode.

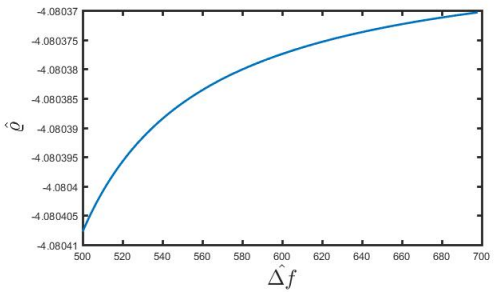
Figure 5 (a) describes the result in buck condition of the SEPIC converter. This result explains that with the minor change in $\Delta C_2$the value of change in output voltage ripples (ϱ) changes. It means how much$\Delta C_2$is increased, so the (ϱ) decreases smoothly. Figure 5 (b) explains that the change in OVR (ϱ) with respect to switching frequency. Figure 5 (b) describes that the (ϱ) rises, when the switching frequency increases from 500 to 600 then it moves with slight change. In Figure 5 (c), not only the value of variable capacitor is changed but also the values of switching frequency are varied to produce present the simultaneous effect of both capacitance and switching frequency change. In Figure 5 (d), the resultant OVR of SEPIC in boost condition are presented with variation of capacitor value that the change ΔC_2in output voltage ripples (ϱ) also changes. It means how much $\Delta C_2$is increased so; the (ϱ) also decreases smoothly. Figure 5(e) explains that the change in OVR (ϱ) related to the switching frequency in boost mode. This process has the same values but slightly changes the value of switching frequency instead of variable capacitor. This figure describes that the (ϱ) rises when the switching frequency is increased from 500 to 680 then it moves with slight change (almost constant). In Figure 5 (f) not only changes in the value of variable capacitor but also change in switching frequency are shown. In this process, remaining values are the same but with the slight variations in the variable capacitor and switching frequency values. In this Figure, it is noted that the change in OVR (ϱ) also varies with respect to switching frequency and variable capacitor ΔC_2, at the start it produces a tremendous change in OVR (ϱ) from -2 to -1.5 but gradually after this change grows in or and there is no the change in ovr(ϱ) after -1.5.

B. IISM-CCM

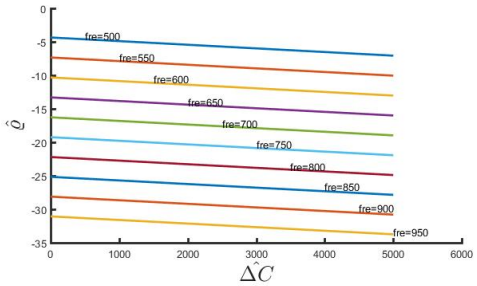
In buck condition of the SEPIC converter, Figure 6 (a) describes the change in OVR (ϱ) with respect toΔC_2which is a variable capacitor. This result is compatible with the minor variation in $\Delta C_2$the change in output voltage ripples (ϱ) also results which suggests with improved $\Delta C_2$the (ϱ) is also minimized. Figure 6 (b) explains the change in OVR (ϱ) with the variation in switching frequency. In this result, it is clear that by decreasing the switching frequency, the change in OVR (ϱ) decreases. Clearly, increase the switching frequency the (ϱ) is diminishing. In Figure 6 (c) shows not only change in variable capacitor but also variation in the value of switching frequency. This Figure commensurate that how much change in switching frequency causes the change in OVR (ϱ)to occur. This Figure categorically defines that the change in OVR (ϱ) is reduced by increasing the value of switching frequency and variable capacitor. In boost condition of SEPIC converter, Figure 6 (d) describes the change in OVR(ϱ) with respect to ΔC_2, which is a variable capacitor. This result is compatible with the minor variation in $\Delta C_2$the change in output voltage ripples (ϱ) is also changing means with the improved$\Delta C_2$the (ϱ) is also minimized. increasing the switching frequency and variable capacitor.



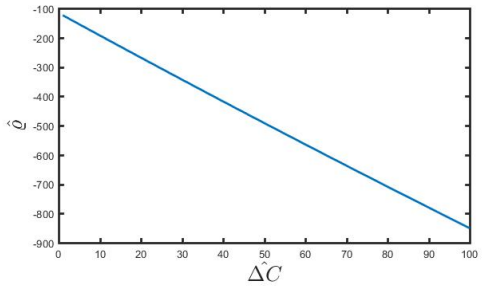
(a) Graph of Variable Capacitor



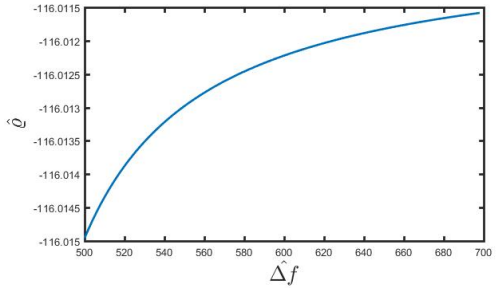
(b) Graph o
f Variable switching frequency



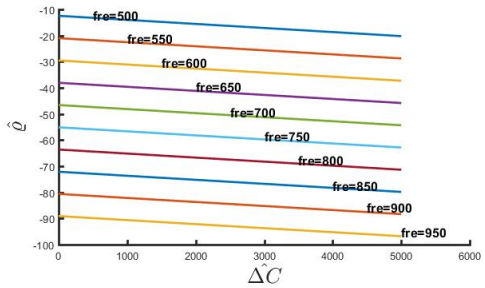
(c) Graph of Variable Capacitor and switching frequency



(d) Graph of Variable Capacitor



(e) Graph of Variable switching frequency



(f) Graph of Variable Capacitor and Switching frequency

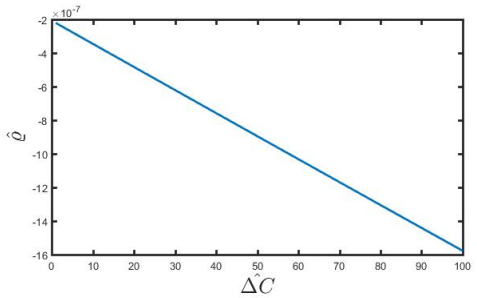
Figure 6. change in output voltage ripple (ϱ) of buck and boost modes in IISM-CCM of SEPIC converter. (a) reports the result of a variable capacitor, (b) defines the result of a variable switching frequency and(c) represents the result of variable capacitor and switching frequency in buck mode while (d) states the result of a variable capacitor, (e) narrates the result of variable switching frequency and (f) defines the result of a variable capacitor and switching frequency in boost mode.

Figure 6(e) explains the change in OVR (ϱ) with the variation in switching frequency. In this result, it is clear that by varying the switching frequency incrementally the change in OVR (ϱ), is decreased. With the increase in the switching frequency the change in OVR is improving. Figure 6 (f) shows not only change in variable capacitor but also changes in switching frequency. This Figure commensurate that how much change in switching frequency and capacitor will cause the change in OVR (ϱ) to appear. This Figure depicts that the change in OVR (ϱ) is decreasing by.

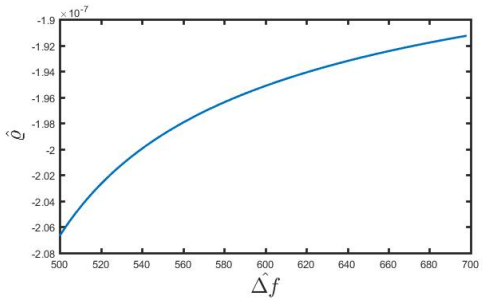
C. IISM-DCM

In buck condition of the SEPIC converter, Figure 7 (a) describes the change in OVR i.e.(ϱ)with respect toΔC_2. Figure 7 (b) explains the change in OVR (ϱ) with the variation in switching frequency. In this result, it is clear that by decreasing the switching frequency, the change in OVR i.e. (ϱ) decreases. In Figure 7 (c) not only the effect of change in capacitor value

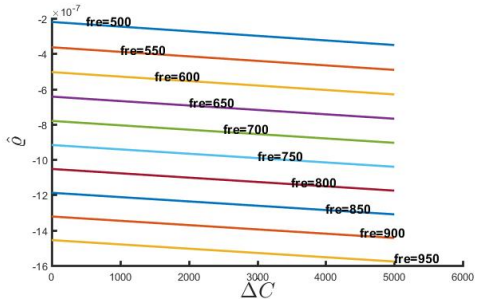
but also variation in the value of switching frequency is presented. This Figure commensurate that change in capacitor value and switching frequency causes the change in (ϱ) to occur. This Figure categorically defines that the change in OVR i.e. (ϱ) is reduced by increasing the value of switching frequency and variable capacitor. In boost condition of SEPIC converter, Figure 7 (d) describes the change in OVR (ϱ) with respect to ΔC_2, which is a variable capacitor. This result shows that with the variation in $\Delta C_2$the change in output voltage ripples i.e. (ϱ) also changes means with the increased the(ϱ) is further minimized. Figure 7 (e) explains the change in OVR (ϱ)with the variation in switching switching frequency. In this result, it is clear that by varying the switching frequency incrementally the change in OVR (ϱ), is decreased. With the increase in the switching switching frequency the change in OVR is improving.



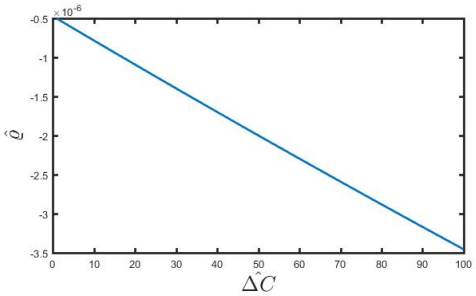
(a) Graph of Variable Capacitor



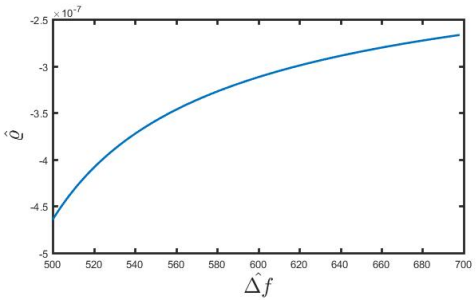
(b) Graph of Variable switching frequency



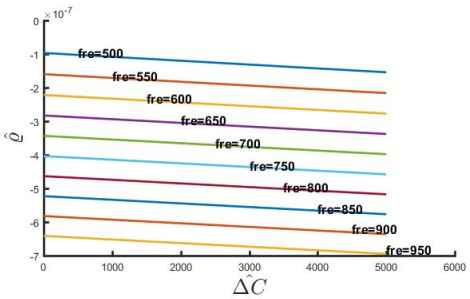
(c) Graph of Variable Capacitor and switching frequency



(d) Graph of Variable Capacitor



(e) Graph of Variable switching frequency



(f) Graph of Variable Capacitor and switching frequency

Figure 7. change in output voltage ripple (ϱ) of buck and boost modes in IISM-CCM of SEPIC converter.(a) reports the result of a variable capacitor, (b) defines the result of a variable switching frequency and(c) represents the result of variable capacitor and switching frequency in buck mode while (d) states the result of a variable capacitor, (e) narrates the result of variable switching frequency and (f) defines the result of a variable capacitor and switching frequency in boost mode.

Figure 7 (f) shows not only change in variable capacitor but also changes in switching frequency This Figure commensurate that how much change in switching frequency and capacitor will cause the change in OVR (ϱ) to appear. This Figure depicts that the change in OVR (ϱ) is decreasing by increasing the switching frequency and variable capacitor.

5. Conclusion

The analysis of results concludes that output voltage ripple is dependent on the values of circuit elementsi. e. capacitor and inductor. Moreover, the switching frequency can also play an effective role in minimizing the OVR. The decrease in OVR in all modes are minimized except Complete Induction Supply mode in Continuous Conduction Mode (CISM-CCM). Where increase in capacitor value and switching frequency results into an increase in the OVR in boost mode.

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