Regulated Telescopic OTA Optimization for Mobile WiMAX Applications. Nano CMOS OTA Performance Prediction Through Bisquare Weights Method

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Abstract: This paper presents the design of a high performance Regulated Telescopic Operational Transconductance Amplifier (OTA) for low power and high speed sigma-delta modulator for Mobile WiMAX Applications. Indeed, the Regulated Telescopic OTA is an enhanced DC gain Telescopic circuit with the gate voltage of the cascode transistor is controlled by a feedback amplifier. An algorithmic driven methodology is developed ending to the optimal transistor geometries. Moreover, the proposed OTA was post-layout simulated for some process corners, temperature variation and Monte-Carlo analysis. The post-layout simulation results have achieved a DC gain of 66dB, a large GBW of 862MHz with a phase margin of 58degrees with only 6.24mW power consumption. In addition, the use of a robust Bisquare Weights (BW) method is investigated to predict the Regulated Telescopic OTA performance for new generation systems. Then, the impact of Nanometer CMOS on Regulated Telescopic OTA design is highlighted. It shows the potentialities of future CMOS processes to provide high speed and high performance OTA circuit.

Keywords: Regulated Telescopic OTA design; Heuristic optimization; DC gain; Bisquare Weights method; nanometer CMOS; predicted OTA performance

1. Introduction

The growing demand for high-speed and high-precision analog integrated circuits dictates stringent design specifications for the amplifiers which are the basic building blocks for numerous applications. In fact, high performance analog-to-digital converters (ADCs) require OTA circuit with very high DC gain and gain-bandwidth product (GBW), to meet both accuracy and fast settling requirements of the systems [1]. In addition, high-gain amplifiers use cascode structures or multi-stage designs with long channel length transistors biased at low current levels, while, high-bandwidth amplifiers use single-stage designs with short channel length transistors biased at high current levels [2]. Telescopic and folded-cascode structures are two common structures for single-stage OTAs. Two main drawbacks of the first one are low input common mode range and large voltage headroom in output. The main disadvantage of the folded one is that the power consumption is high and the GBW is low [3].

The OTA circuits can be achieved by exploiting the CMOS which is the preferred process for integrating systems on a chip. The CMOS process has been scaled according to Moore's Law, where the number of transistors on chips has grown at a faster rate in recent years [4]. Since process variations severely affect the characteristics of MOSFETs at the nanoscale, the prediction of analog circuit performances in sub-nm technologies is necessary to evaluate its capacities when designed using the future Nano-CMOS technology. In fact, performance estimation is a big challenge for analog circuit designers. Several approaches have been developed for efficient estimation. In fact, the least squares method is a standard method of adjustment which is elaborated by Legendre and Gauss [5]. It aims to get a smooth curve that fits the data points, x1…xi and it minimizes the sum of squared residuals [6]. The BW method is the most commonly used technique which is more accurate, yielding better predictions [7].

The objective of this work is to design a Regulated Telescopic OTA with a high DC gain

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and large GBW that satisfy the WiMAX application requirements. To achieve the targeted performance objectives, a Heuristic method used ending to the optimal OTA performance. Since the performance of this basic element circuit is closely related to the transistor scaling, we focus on evaluating the capacity of Regulated Telescopic OTA when designed using Nanometer CMOS process. We use the robust BW method to predict the Regulated Telescopic OTA performance during technology scaling.

The remaining of this paper is organized as follows. The design of the Regulated Telescopic OTA circuit is introduced in section 2. Analytical equations are investigated. The Heuristic method is presented in this section, together with optimized performance for the Regulated Telescopic OTA. Section 3 presents the post-layout simulation as well as process corners, temperature variation and Monte-Carlo analys is results. The predicted and optimal performance of the Regulated Telescopic OTA for future process is described in section 4. Finally, the main conclusions of this study are drawn in section 5.

2. Regulated Telescopic OTA optimization

Due to scaling of CMOS process technologies, lower supply range, and stronger focus on system-on-chip integration, analog design becomes more and more challenging. The operational transconductance amplifier, being an integral part of most analog systems, needs to address the stringent specifications on gain, bandwidth, linearity, noise and supply as well as stability [8]. The aim of this work is to design a Regulated Telescopic OTA instead of the conventional Telescopic OTA. In order to get more DC gain without changing the gain-bandwidth product, Telescopic OTA with the gate voltage of the cascode transistor being controlled by a feedback amplifier [9]. The feedback is applied around the cascode transistor in order to enhance the gain. This feedback is in fact a parallel-series, causing the output impedance to increase with the amount of feedback gain. The gain rises with the same amount. So, the gain boosting adds another gain enhancement at low frequencies, without altering the GBW [10]. Figure 1 reveals the proposed Regulated Telescopic OTA. Despite, adding a feedback amplifier, the voltage swing of the Regulated Telescopic OTA at the output node was decreased and the layout area was raised, compared to the Telescopic OTA circuit.

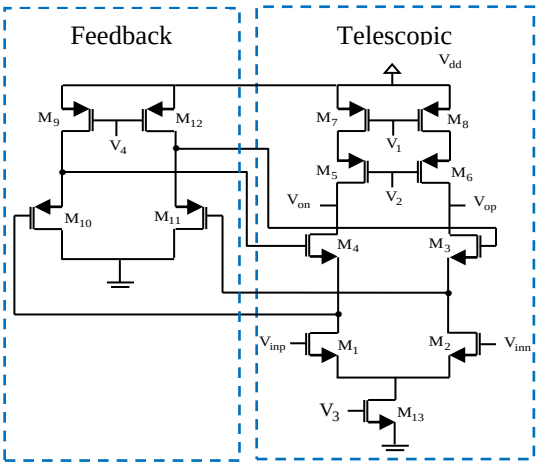

Figure 1. Schematic of the Regulated Telescopic OTA

Design of CMOS analog circuits are very significant in electronic system design. Day by day design complexity of electronic circuits is increased. So that, the optimization procedures should be automatic using greater precision. The key problems concern with electronic design automation are robustness and cost. Usually, optimization is a very exciting and time-consuming task with many conflicting benchmarks and a wide range of design parameters. The proposed OTA can be designed using gm/ID methodology introduced by Flandre and Silveira

[11]. However, we can only optimize the characteristics containing gm/ID parameter within expression's models [12].Thus, an alternative design approach is developed in this paper. It presents an optimization tool based on Heuristic algorithms [13]. We fixed our choice in this step of the AMS 0.35µm CMOS process. The Regulated Telescopic OTA optimization is based on maximizing the DC gain (A_v), the GBW and the common mode rejection ratio (CMRR), and minimizing the input referred noise ($V_{T,in}^2$)and the silicon area of the whole OTA circuit. The objective function to maximize can thus be presented as follows:

$$F_o = \theta_1 A_v + \theta_2 GBW + \theta_3 CMRR + \frac{\theta_4}{{V_{T,in}}^2} + \frac{\theta_5}{\sum W_i L_i} \quad (1)$$

Where $\theta_1,\ldots, \theta_5$ are positive coefficients used for normalization.

The first step in the optimization is the expression of the different criteria by a technology dependent model. For accurate modeling, a small signal analysis of the Regulated Telescopic OTA is carried out to explicit the different characteristics intended to optimize. From Regulated Telescopic OTA architecture presented in Figure1, the output resistance equation is given by the following equation:

$$R_{out} = ((gm_4 + gm_{10})ro_4(ro_{10}//ro_9)ro_1)//(gm_5 ro_5 ro_7) \quad (2)$$

Where g_{mi} and ro_i are respectively the transconductance of M_i transistor for i = (4, 5, 10) and the drain-source resistance of M_i device for i = (1, 4, 5, 7, 9,10). As a result, the open loop gain of the Regulated Telescopic OTA circuit is expressed as:

$$A_v = G_m R_{out} = g_{m1}((gm_3 + gm_{10})ro_3(ro_{10}//ro_9)ro_1)//(gm_5 ro_5 ro_7) \quad (3)$$

The GBW is then given by:

$$GBW = \frac{g_{m1}}{2\pi(C_{DB3}+C_L+C_{GD3})} \quad (4)$$

Where C_{DB3} and C_{GD3} are respectively the bulk drain capacitance and the drain gate capacitance of the M_3 transistor and C_L is the capacitance at the output node. The common mode rejection ratio (CMRR) can be approximated as:

$$CMRR = \frac{2ro_{13}g_{m1}(g_{m5}ro_5 ro_7)//(g_{m3}ro_3 ro_1)}{ro_7} \quad (5)$$

The input referred thermal noise voltage of the Regulated Telescopic OTA can be expressed as:

$$\overline{V_{in,th}}^2 = 4KT\left(2\frac{2}{3g_{m1,2}} + 2\frac{2g_{m7,8}}{3{g_{m1,2}}^2}\right) \quad (6)$$

Where K is the Boltzmann's constant and T is the temperature. The input referred Flicker noise voltage of the Regulated Telescopic OTA can be written as:

$$\overline{V_{in,1/f}}^2 = 2\frac{KFN}{C_{ox}(WL)_{1,2}GBW} + 2\frac{KFP}{C_{ox}(WL)_{7,8}GBW}\frac{{g_{m7,8}}^2}{{g_{m1,2}}^2} \quad (7)$$

Where KFN and KFP are the Flicker noise coefficients of NMOS and PMOS transistors respectively. C_{ox} is a constant for a given process. W and L represent the transistor sizes.

The heuristic and all constraints on each MOS transistor forming the Regulated Telescopic OTA were mathematically modelled, and developed in C++ [14]. Thus, this program allowed us to teach high performance of OTA circuit. This approach was followed in several analog circuit designs and has produced promising results [15]. In fact, the heuristic algorithm used for optimizing the Regulated Telescopic OTA performances is essentially a random process. As shown in Figure 2, the mathematical models for both constraints and preliminary conditions to satisfy should be firstly developed. This program gives all possible parameters that are candidates for optimization taking into account their variations range. Secondly, the performance criteria and error sources are mathematically modeled. Afterwards, these models are taken into consideration in the program, and optimal parameters can be randomly selected from among the already calculated parameters. The objective function compilation to minimize or to maximize leads to optimal devices such as width and length values.

The optimization strategy which is essentially a random process, is detailed by the Figure2. Firstly, it initializes the parameters vector, which includes the size of the different MOS transistors interfering in the above analytical expressions. Next, the variable vector is selected and the preliminary requirements are checked. If these requirements are satisfied, then we can go the next step, otherwise, we make another choice. Afterward, we calculate the

objective function. We record the parameters vector, if the objective function value has decreased. In fact, the testing vector is the parameters vector which includes the size of the different MOS transistors (width and length values) interfering in the analytical expressions. Moreover, at the end of heuristic algorithm, We record the new testing vector including the optimized size of the different MOS transistors.

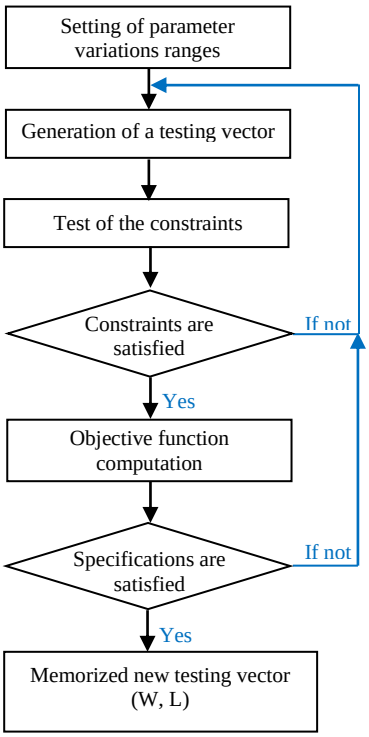

Figure 2. Flowchart of the heuristic

Simulation conditions are such as: the supply voltage is 3.3V and the capacitor load is 1pF. We notice that the optimization algorithm can be done in the same way for other simulation conditions. Table 1 summarizes the optimal device scaling that we get after applying the optimization algorithm. In addition, the designed Regulated telescopic OTA has a gain of 69.15dB and a large GBW of 870MHz as presented in Figure 3. The transistor-level simulated performance is compared to theoretical design in Table 2. It is seen that the optimization procedure is almost satisfactory.

Table 1. Optimal device sizing

Device name	Aspect ratio (µm)
$W_{1,2,3,4}$	800/0.8
$W_{5,6,7,8}$	1100/0.5
W_{13}	590/0.5
$W_{9,12}$	900/0.8
$W_{10,11}$	200/0.8

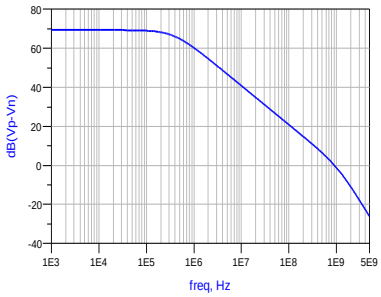

Figure 3. Gain curve

Table 2. Performance comparison

Performance	Theoretical values	Simulated values
DC gain (dB)	77.82	69.15
GBW (MHz)	970	870
CMRR (dB)	57.44	51
Slew rate (V/µs)	395	351
Power consumption (mW)	6.34	6.22

3. Post-layout simulation results

In order to evaluate the proposed Regulated Telescopic OTA design, various post-layout simulations are performed using AMS 0.35µm CMOS process parameters. The output frequency response of the Regulated Telescopic OTA, with 1pF load capacitance, is plotted in Figure 4. The Regulated Telescopic OTA has a DC gain of 66dB, a large GBW of 862MHz and a phase margin of 58 degrees. The Regulated Telescopic OTA performance is summarized in Table 3.

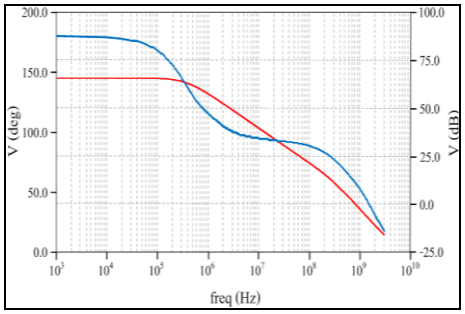

Figure 4. Gain and Phase curve

Table 3. Regulated telescopic OTA performance

Performance	Transistor-level simulation	Post-layout simulation
DC gain (dB)	69.15	66
GBW (MHz)	870	862
Phase margin (degrees)	60	58
CMRR (dB)	51	49.4
Slew rate (V/µs)	±351	±349
Settling time (ns)	14.24	14.3
Output-voltage swing (V)	-1.5 to 1.5	-1.2 to 1.2
Supply voltage (V)	0 - 3.3	0 - 3.3
Power consumption (mW)	6.22	6.24
Layout area (μm^2)	-	(221×202)

The Regulated Telescopic OTA is post-layout simulated for five process corners, namely: Fast Fast (FF), Typical Typical (TT), Fast Slow (FS), Slow Fast (SF) and Slow Slow (SS). Figure 5 shows the process corners post-layout simulation for gain curve. In addition, Table 4 lists the post-layout simulation performance of the Regulated Telescopic OTA for all the process corners. It can be clearly seen that the GBW, the Slew Rate, the settling time and the power consumption vary significantly over the process corners.

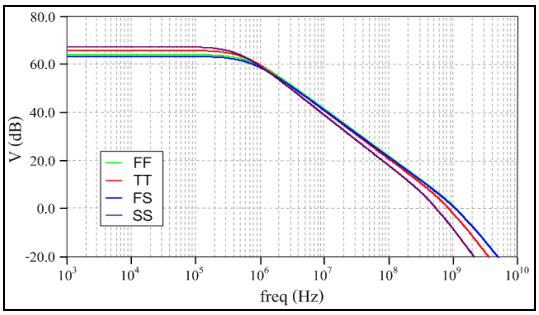

Figure 5. Process corners post-layout simulation for gain curve

Table 4. Post-layout simulation performance of the Regulated Telescopic OTA for all the process corners

Performance	Process Corners				
	TT	FF	FS	SF	SS
DC gain (dB)	66	64.02	63.22	67.32	67.18
GBW (MHz)	862	1090	1082	556	556
Phase margin (degrees)	58	54.86	54.57	61.59	61.57
CMRR (dB)	49.4	48.31	47.96	50.48	50.19
Slew rate (V/µs)	±349	±360	±357	±264.89	±263.84
Settling time (ns)	14.3	13.85	13.97	17.74	17.78
Output-voltage swing (V)	-1.2 to 1.2	-1.17 to 1.17	-1.21 to 1.21	-1.13 to 1.13	-1.14 to 1.14
Power consumption (mW)	6.24	7.75	7.76	5.96	6.08

The proposed OTA was post-layout simulated for temperature variation from -20°C to +100°C. Figure 6 shows the temperature variations effect on the gain curve. Moreover, the post-layout Regulated Telescopic OTA performances for temperature variations are summarized in Table 5. It can be clearly seen that the GBW and the power consumption vary significantly across temperature variation.

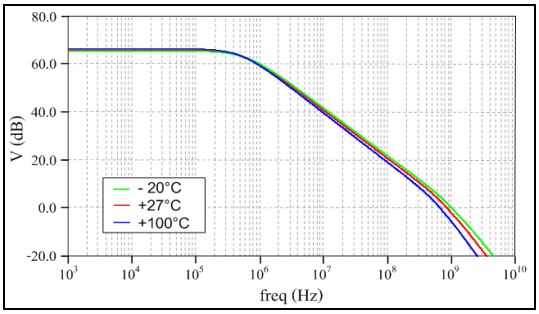

Figure 6. Gain curve with temperature variation from -20°C to +100°C

Monte-Carlo simulations have been performed in order to check how the transistor mismatch affects performance of the Regulated Telescopic OTA circuit. Figure 7 shows the results of a Monte-Carlo simulation with 100 runs performed on the OTA circuit when all significant process parameters are varied by ±10% from their nominal values. As can be seen from the histogram (Figure 7), ±10% process parameters mismatches would result in an

average DC gain of 63.54dB. Hence, the degradation is about 2.46dB. Furthermore, the main results of the Monte Carlo simulations are summarized in Table 6. It shows that the results of Monte-Carlo simulation have low variation from that of post-layout simulation results, except for the power consumption. We are focusing on the abilities evaluation of Regulated telescopic OTA when designed using future upcoming CMOS process. Moreover, we look forward to estimate the proposed OTA performance with process scaling.

Table 5. Regulated Telescopic OTA performance with temperature variation

Performance	Temperature		
	-20°C	+27°C	+100°C
DC gain (dB)	65.91	66	66.11
GBW (MHz)	1048	862	662
Phase margin (degrees)	57	58	60.1
CMRR (dB)	47.67	49.4	51.27
Slew rate (V/µs)	±352	±349	±348
Settling time (ns)	14.28	14,3	14.31
Output-voltage swing (V)	-1.21 to 1.21	-1.2 to 1.2	-1.13 to 1.13
Power consumption (mW)	5.45	6.24	6.75

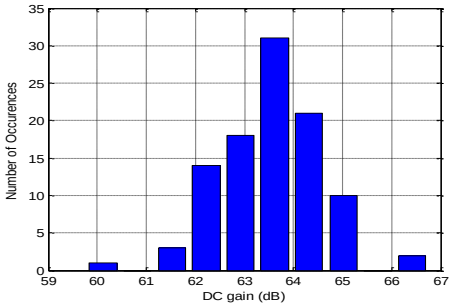

Figure 7. Histogram of 100-run Monte-Carlo simulation showing the effect of ±10% process parameters mismatches on DC gain

Table 6. Results of Monte-Carlo simulation

Performance	Post-layout simulation	Monte-Carlo simulation
DC gain (dB)	66	63.54
GBW (MHz)	862	897
Phase margin (degrees)	58	59.24
CMRR (dB)	49.4	47.44
Slew rate (V/µs)	±349	±344
Settling time (ns)	14.3	14.35
Output-voltage swing (V)	-1.2 to 1.2	-1.12 to 1.12
Power consumption (mW)	6.24	7.44

4. Prediction of the Nano CMOS Regulated Telescopic OTA performance

The aim of analog designers is to minimize the OTA power consumption through Nanometer CMOS processes. We place the accentuation on the prediction of Regulated Telescopic OTA performance using future CMOS processes. As shown in Figure 8, we begin by specifying the process node. Furthermore, we choose the parameters listed in Table7 including supply voltage (V_{dd}), threshold voltage (V_{th}), equivalent electrical oxide thickness (T_{oxe}), channel doping concentration (N_{ch}) etc... that are useful for OTA circuit design [6]. The analytical expressions that characterize the OTA circuit and the Nanoscale technological parameters are then used to apply the optimization process. Finally, the performance of

Regulated Telescopic OTA such as DC gain, GBW, CMRR, Slew rate and power consumption are predicted and optimized.

Table 7. List of Nanoscale technological parameters

Process nodes (nm)	65		90		130		180		250	
Data sources	INTEL[04]		TSMC[02]		INTEL[01]		TSMC[09]		TSMC[09]	
Device Type	N	P	N	P	N	P	N	P	N	P
V_{dd} (V)	1.2		1.2		1.4		1.8		2.5	
V_{th} (V)	0.28	-0.24	0.29	-0.22	0.33	-0.25	0.37	-0.38	0.37	-0.52
T_{ox} (nm)	1.85	1.95	2.05	2.2	2.15	2.3	4.1	4.1	5.7	5.7
N_{ch} (e^{18} cm^{-3})	5	5	3.5	3.5	2.5	2.5	0.23	0.41	0.23	0.41

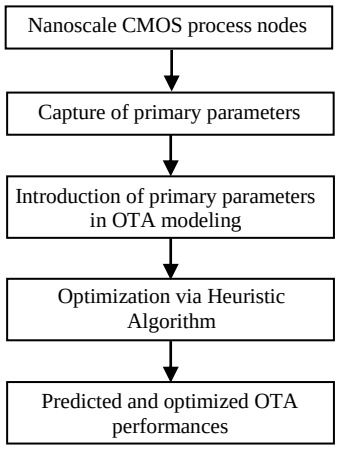

Figure 8. Synoptic of Nano CMOS OTA performance prediction

A. Prediction method process

The Bisquare Weights prodective method needs (xi, yi) scatter as long as a monotony combination of x and y parameters is set, in order to reach a smooth scaling [16, 17]. x and y parameters define respectively the process nodes and Regulated Telescopic OTA performance. Our object consists of fitting linear or non-linear models to data using the robust BW method from 45nm to 22nm process nodes.

Firstly, we use the Matlab command "cftool". We are often confronted with the task of determining the best model among various proposed alternatives, before fitting the scatter set (xi, yi). In order to choose the best fit, we compare different fit results, including the fitted coefficients and goodness of fit statistics. Moreover, the graphical and numerical fit results should be considered such as the residuals, the prediction bounds, the goodness of fit statistics and the confidence bounds. Afterwards, when the fit model is fixed, we extrapolate it to predict the Regulated Telescopic OTA performance from 45nm to 22nm process nodes. Finally, we plot both the predicted results and the data. We take as an example, residuals graphical display of different model fits as given in Figure 9. In fact, we fit (xi, yi) data with polynomial, exponential and power model fits. The residual for power model appears randomly scattered around zero proving that the model fit the data well. In addition, the polynomial and exponential models are not suitable fit for the data because the residuals are systematically negative for much of the data range. Besides, the numerical fit results are summarized in Table8. In fact, the power model represents the best fit since the associated SSE and RMSE values are the lowest.

To prove the robustness of BW method, we compared it with another method called least-square (LS) method. In fact, the LS method is a standard approach elaborated by Legendre and Gauss [5]. As shown in Figure 10, we are fitting the data with the power model using the LS

and the BW methods. From this figure, it can be seen that the use of BW method results in a smooth and accurate fitting.

Table 8. Numerical fits results

General model fit	Coefficients values (with 95% confidence bounds)	Goodness of fit statistics			
		SSE	R-sq	Adj-R-sq	RMSE
Linear polynomial: f(x)=ax+b	a= 0.039 [0.025, 0.052] b= 65.15 [62.46, 67.84]	5.25	0.94	0.92	1.14
Power: $f(x)=ax^b$	a= 44.98 [43.77, 46.18] b= 0.093 [0.088, 0.098]	0.14	0.99	0.99	0.19
Exponential: f(x)=aexp(bx)	a= 65.54 [62.78, 68.29] b= 0.00052 [0.00033, 0.00072]	6.4	0.92	0.91	1.26

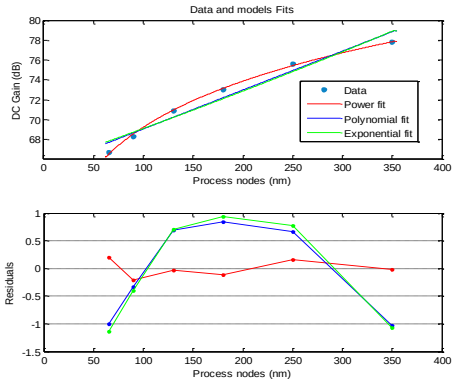

Figure 9. Graphical fits results

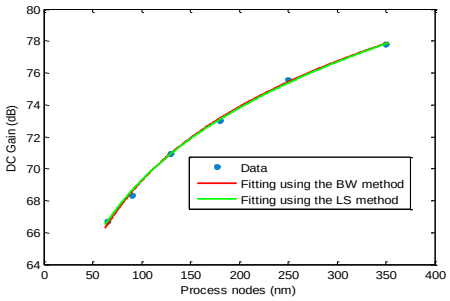

Figure 10. Fitting using both of the LS and the BW methods

B. OTA performance prediction for Nano CMOS process

High speed transistor can be provided, when analog designers move into a Nano CMOS process. The GBW varies between 0.97GHz and 6.61GHz, it was noticed that the GBW of the Regulated Telescopic OTA was improved as shown in Figure 11. The GBW of upcoming transistor is continuously growing up with length decreasing of the transistor channel. The intrinsic gain of a transistor was decreased, hence, Figure 12 and Figure 13 prove the decline of Regulated Telescopic OTA DC gain and CMRR respectively. A gain-speed trade-off must be made in Nanometer CMOS process when faster speed and less gain are got from a single transistor. The Slew rate was decreased as shown in Figure 14, due to the strong rise of transconductance during the scaling process. The device characteristics become more sensitive to variations in the reduced channel length, making the OTA design tasks delicate. The shrinking of dimensions and supply voltage of the Regulated telescopic OTA circuit reduce significantly the power consumption. Figure 15 reveals the possible decrease of Regulated Telescopic OTA power consumption from 6.34mW to 1.75mW. During Nanoscale process, in

spite of the reduction of DC gain, Regulated Telescopic OTA circuit presents acceptable DC gain useful for high speed applications.

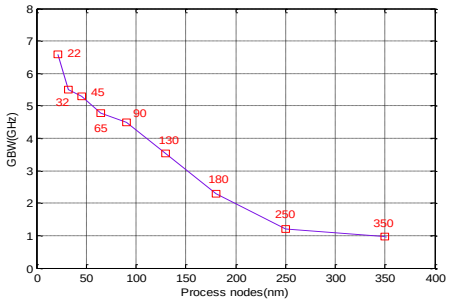

Figure 11. The scale of GBW

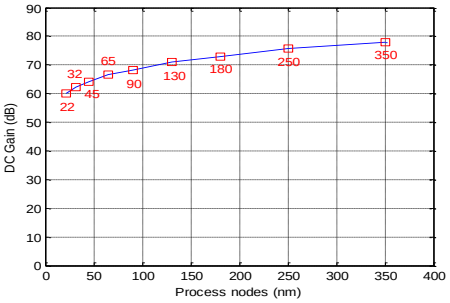

Figure 12. The scale of DC Gain

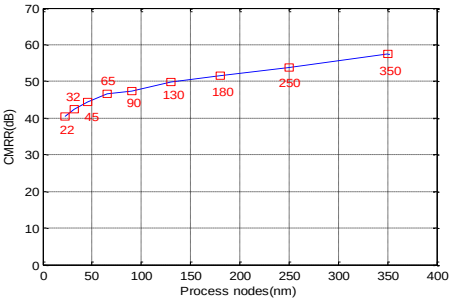

Figure 13. The scale of CMRR

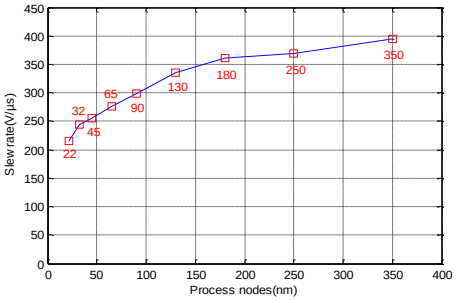

Figure 14. The scale of Slew rate

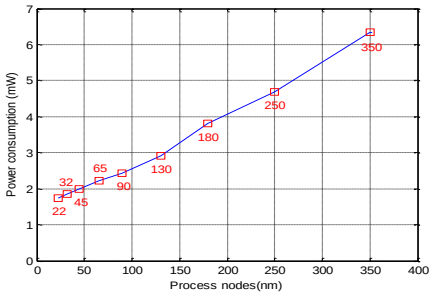

Figure 15. The scale of power consumption

C. Evaluation of bisquare weights method

In order to approve the robustness of the bisquare weights method, we interpolate the Nano CMOS Regulated Telescopic OTA Performances for 180nm process nodes. In addition, we focus on comparing the interpolated OTA Performances with transistor-level simulation of the OTA circuit. The output frequency response of the Regulated Telescopic OTA for 180nm process nodes is plotted in Figure 16. The Regulated Telescopic OTA has a DC gain of 67.3dB, a GBW of 1.99MHz. Table 9 summarizes the verification of 180nm Bisquare Weights method with OTA transistor-level simulation. Moreover, the relative error given by Table 9 can be written as:

$$\text{Relative error} = \frac{\text{real value} - \text{measured value}}{\text{real value}} \quad (8)$$

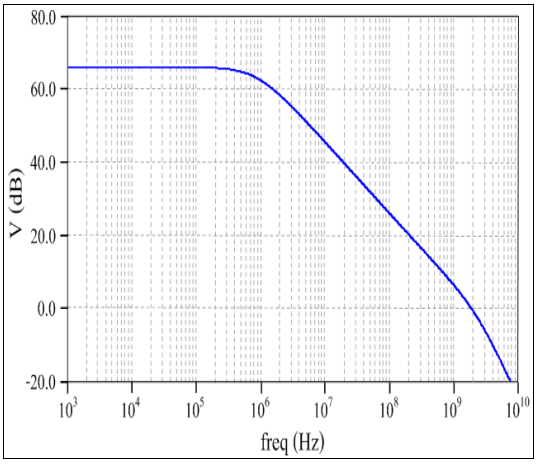

Figure 18. Gain curve for 180nm process nodes

Table 9. Verification of 180nm Bisquare Weights method with OTA transistor-level simulation

	BW method	transistor-level simulation	Relative error (%)
DC gain (dB)	73.14	65.90	10.9
GBW (MHz)	2.18	1.99	9.5
CMRR (dB)	51	46.43	9.8
Slew rate (V/μs)	360	330	9
Power consumption (mW)	3.69	3.65	1

The real value and the measured value represent, respectively the values given by OTA transistor-level simulation and BW methods. We conclude that the values of Regulated Telescopic OTA Performance interpolated with the BW method is approximately close to those given by the transistor-level simulation with a deviation of less than 11%. Therefore, a

satisfactory agreement between interpolated and transistor-level simulation of OTA performance is achieved. Then, the robust Bisquare Weights method proves the physicality and scalability of the performed interpolation. Otherwise, we verified the effectiveness of Bisquare Weights method by extrapolation. In fact, the values of Regulated telescopic OTA performance, predicted by BW method from 45nm to 22nm process nodes, have been carried out. Table 10 summarizes the estimated performance of the proposed OTA in comparison with other OTAs circuit presented recently. Relying on this comparison table, the values of OTA performance predicted with BW method are approximately close to those given by the literature. Therefore, the BW method proves the scalability of its extrapolation.

Table 10. Comparisons of estimated OTA Performance with other literatures

Performance	This work			[18]	[19]	[20]
Process (nm)	45	32	22	32	45	50
Supply Voltage (V)	1	0.96	0.92	1	1.3	1
DC gain (dB)	64.2	62.16	55.9	53.43	57.83	57.15
GBW (GHz)	5.3	5.5	6.6	0.741	0.074	0.604
CMRR (dB)	44.29	42.32	40.36	-	-	-
Slew rate (V/µs)	255	245	215	-	-	-
Power consumption (mW)	2	1.85	1.75	-	0.042	0.56

5. Conclusion

In this work, the design and implementation of a Regulated Telescopic OTA intended for use in Sigma-Delta modulator for Mobile WiMAX Applications were achieved. In fact, our design technique aimed at keeping an enhanced DC gain Telescopic OTA. For this reason, the telescopic OTA circuit with the gate voltage of the cascode transistor is controlled by a feedback amplifier. Moreover, an efficient optimization tool based on Heuristic algorithms was developed ending to the optimal transistor geometries. Behavioral transistor-level and post-layout simulations were presented. Then, we investigated both the process corners and the temperature variation as well as the Monte-Carlo analysis for Regulated Telescopic OTA to provide a better prediction for the experimental performance. The post-layout simulation results achieve high open-loop DC gain of 66dB and large measured GBW of 862MHz. The power consumption is approximately equal to 6.24mW under 3.3V supply voltage. In addition, we focused on the use of the Bisquare Weights method to predict the Regulated Telescopic OTA performances using upcoming CMOS Nanoprocess. The Heuristic program plays a key role in optimizing the predicted performance of Regulated Telescopic OTA. The CMOS scaling down leads to not only make high performance OTA, but also overcome several implementation difficulties. Future works will involve the use of the BW method to predict the Sigma-Delta modulator performance for ADCs used in Mobile WiMAX receivers.

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