Low-Ripple High-Ratio DC-DC Converter Based on Multilevel-Multiphase Modified Cuk Converter Topology

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Abstract: A multilevel-multiphase topology based on modified Cuk converter is proposed in this paper. This paper employs the combination of multiphase and multilevel topology which is applied to the modified dc-dc the Cuk converter serves as the fundamental cell topology to achieve low-ripple high-ratio DC-DC converter. The multiphase approach will generate smaller current ripples in the input and output sides so it will be beneficial for ripple-prone sources or load, for example photovoltaic panel or battery. Meanwhile, the multilevel approach will generate high ratio amplification for input voltage, provided by PV panel or battery, to reach typical 380-400VDC in the output voltage which is suitable for DC microgrid applications. A four levels multilevel-multiphase modified Cuk converter topology is successfully developed. The derivation of the mathematical expression of the voltages applicable to the proposed converter is conducted. Loss analysis is conducted to observe the contributing factor of losses to the total efficiency is conducted. A double-loop control system is proposed for the proposed converter to achieve the desired reference operation point for various conditions. It can be demonstrated that the proposed converter generates high ratio total output voltage while maintaining notably small current ripple. Simulation and experiment are conducted to verify the performance of the proposed converter.

Keywords: Modified Cuk Converter, Multiphase, Multilevel, High Voltage Ratio, Power Loss Fraction, Current Ripple, Efficiency, Closed-Loop, Control System

1. Introduction

Primary energy in electricity generation in most regions of Indonesia is still dominated by fossil energy with a mix of 67.21% for coal, 15.96% for gas, and 2.73% for fuel oil in 2022. Meanwhile, the New and Renewable Energy (NRE) mix was only 14.11% in the same year. Meanwhile, the Indonesian government set target for the NRE mix in 2025 is at 23% and in 2030 at 31%. Indonesia has abundant NRE potential, especially in solar energy, estimated about 207.8 Gw as recorded in 2021. So that by maximizing NRE, especially solar energy, the NRE mix target can be achieved. One of implementation that can be realized is by utilizing a DC microgrid system. One of the most important components in the DC microgrid system is the DC-DC converter. Due to the low voltage output of Photovoltaic (PV) panel by nature which is in the range of 12-to-48 VDC while the demand of electricity at the residential level is 220VAC, therefore 380-400 VDC is required in the input side of the DC-AC converter. On the other hand, either PV panel or battery is prone to the current ripple generated by power electronics converter [1]-[9]. This encourages the existence of DC-DC converters that can meet these needs, to increase the output voltage of PV panel, or battery, by a high ratio using multilevel topology and having low current ripple using multiphase topology.

The application of DC-DC Cuk converters is the main topic of this study. One significant advantage of the Cuk converter is its ability to achieve a higher voltage ratio while ensuring continuous current flow on both the input and output sides.. However, there is a disadvantage, though, with reverse polarity on the output side. To solve the polarity issue, a modified Cuk converter is suggested in this study. Furthermore, a multiphase topology is proposed in this study to lower the current ripple. To achieve a higher voltage ratio, a multilevel topology is also proposed.

Received: March 9th, 2024. Accepted: August 26th, 2024
DOI: 10.15676/ijeei.2024.16.3.1

One method for lowering current ripples in a power converter is by employing multiphase topology. The converter's arms are controlled by shifting the phase of Carrier wave signals, consequently current cancellation will happen, which lowers the ripple in the input org the output side. However, the use of this topology will add components to the converter in the price of reduction of current ripple [10]-[14]. An output voltage increase from multilevel topology can be more than that from conventional converters. The Modular Multilevel Converter (MMC) topology is the multilevel topology that is currently in widespread use. One advantage of this topology is that the converter's cell may be made modular so that all its module parts have the same rating, the same duty cycle value control, and can be more easily scaled to provide the desired voltage. However, this topology has drawbacks of its own, including the need for multiple levels of converters to achieve a higher output voltage value and sensitivity to variations in the specifications of the converter's component parts [15]–[18]. The advantages of these two topologies—multiphase topology and multilevel topology—can improve the DC-DC converter's ability to achieve a high voltage ratio and while maintaining lower current ripple.

This research paper proposes the combination of multiphase and multilevel topology which is applied to the modified dc-dc Cuk converter as the basic cell topology. The multiphase topology will generate smaller current ripples in the input and output sides so it will be beneficial for ripple-prone source or load, for example photovoltaic panel or battery. Meanwhile, the multilevel topology will generate high ratio amplification for input voltage, provided by PV panel or battery, to reach typical 380-400VDC in the output voltage which is suitable for DC microgrid applications. The derivation of the mathematical expression applicable to the proposed converter will be discussed in this paper.

This study will also provide the experimental results for both the open loop and the closed loop of the proposed converter. The effectiveness of the implementation of the multiphase topology will be demonstrated by the open-loop experiment that shows the generated ripple current is notably small. The observation of power loss fraction and efficiency of the converter will also be provided by the open-loop experiment. Furthermore, a closed-loop experiments system based on double-loop control scheme is proposed to achieve the desired reference operation point for various conditions.

2. Proposed Converter

A. Conventional Cuk Converter

The conventional Cuk converter integrates two standard DC-DC converter topologies, specifically the Boost and Buck converters, or in reverse order. The circuit diagram of the Cuk converter is illustrated in Fig. 1[19]. The graph in Fig. 2 illustrates the Cuk converter's l, assuming that there is a continuous flow of current on both the input side (Id) and the output side (Io). It is also assumed that the output side (Co) and center side capacitor (C) are big enough to store energy and generate a constant voltage.

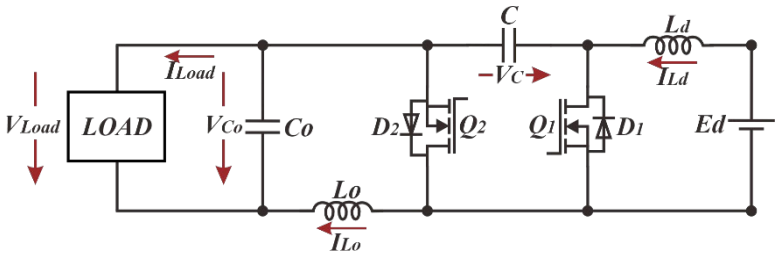


Fig. 1. Conventional Cuk Converter

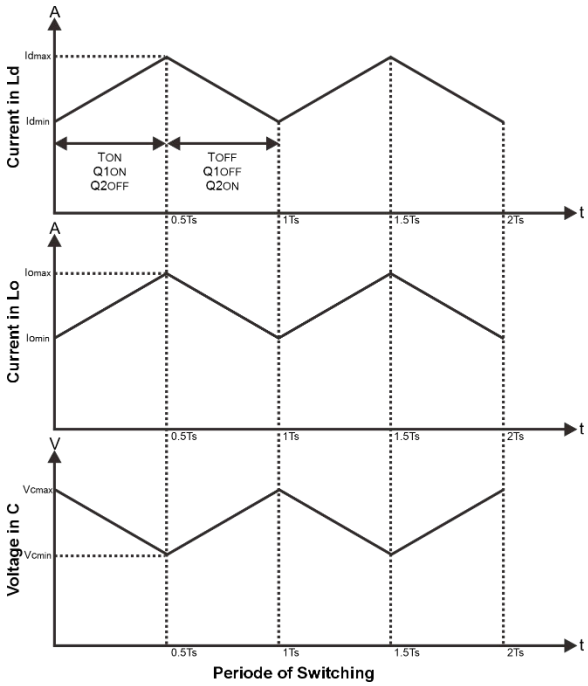


Fig. 2. Operating Principle of the Cuk Converter

The equation for the output voltage Vo in the Cuk converter can be derived based on the previously explained operating principle, as shown in Eq. (1) [19].

$$\frac{V_o}{E_d} = \frac{\alpha}{1-\alpha} \tag{1}$$

For transistor Q1, the duty cycle value has the condition as shown in Eq. (2).

$$\alpha = \frac{T_{ON}}{T_s} \tag{2}$$

From the conventional Cuk converter, these features can be summed up as follows [19].

1. The current ripple is reduced because both the input and output currents are continuous.
2. Vo (output voltage) can fluctuate above or below Ed (input voltage).
3. Vo (output voltage) polarity is inverted in comparison to Ed (input voltage), potentially adding complexity to the implementation of the Cuk converter.

B. Modified Cuk Converter

The Cuk converter, with its continuous input and output currents, offers a significant advantage over other DC-DC converters. Compared to converters like the Boost and Buck, the Cuk converter can achieve a lower generated current ripple. However, the reverse voltage polarity and greater duty cycle value required by this Cuk converter compared to the Boost converter is a drawback. To fix these issues, the Cuk converter's output terminal can be moved to fix these issues. Thus, a modified Cuk Converter is proposed as shown in Fig. 3, by using this modified topology the voltage polarity issue is fixed and a transistor in the switch allows for the bidirectional power[19].

Based on the operating principle used is the same as in Fig. 2, this gives the expression of voltages as shown in Eq. (3)-(4) [19].

$$\bar{v}_o = \frac{\alpha E_d}{1-\alpha} - \frac{V_Q}{1-\alpha} - \frac{R_d(1-2\alpha+2\alpha^2)+R_Q}{(1-\alpha)^2} I_L \tag{3}$$

$$\bar{v}_L = \frac{E_d}{1-\alpha} - \frac{V_Q}{1-\alpha} - \frac{R_d(1-2\alpha+2\alpha^2)+R_Q}{(1-\alpha)^2} I_L \tag{4}$$

This converter offers the following advantages over other DC-DC converters [19].
1. Higher voltage gain at the same duty cycle.
2. The reverse polarity problem has been fixed.
3. The resulting efficiency is higher because the converter does not process all of the power.

Extensions and variations of the modified Cuk circuit of Fig. 3 can be made by changing the position of the inductor. Therefore, different modified Cuk converter circuits are obtained as shown in Fig. 4[19].

Based on Fig. 4, Eqs. (5) and (6) provide formulas for the output voltage drop for each circuit. Eq. (5) represents the voltage drop in the circuit shown in Fig. 4(a), and Eq. (6) represents the voltage drop in the circuit shown in Fig. 4(b) [19].

$$\bar{v}_L = \frac{E_d}{1-\alpha} - \frac{V_Q}{1-\alpha} - \frac{R_d(2-2\alpha+\alpha^2)+R_Q\alpha+R_D}{(1-\alpha)^2} I_{Lo} \tag{5}$$

$$\bar{v}_L = \frac{E_d}{1-\alpha} - \frac{V_Q}{1-\alpha} - \frac{R_d(1+\alpha^2)+R_Q\alpha+R_D}{(1-\alpha)^2} I_{Ld} \tag{6}$$

The transistor and inductor components are responsible for the voltage losses in the circuits shown in Figs. 3-4. While the voltage losses caused by transistors are identical, the losses induced by inductors vary. This is because the inductor current flowing in the inductor below is greater than that flowing in the inductor above and in the middle. The voltage drops in the circuit shown in Fig. 4(b) is larger than in the other circuits.

C. Multiphase Modified Cuk Converter

By employing a multiphase topology, the modified Cuk converter that was previously described can be developed further. The modified Cuk converter's current ripple can be minimized by the multiphase topology. This development can be employed to the circuits shown in Fig. 3, 4(a) and 4(b), as shown in Fig. 5 [20].

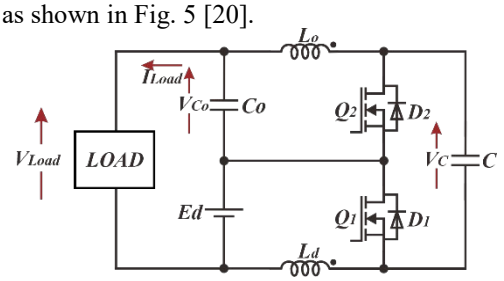


Fig. 3. Modified Cuk Converter

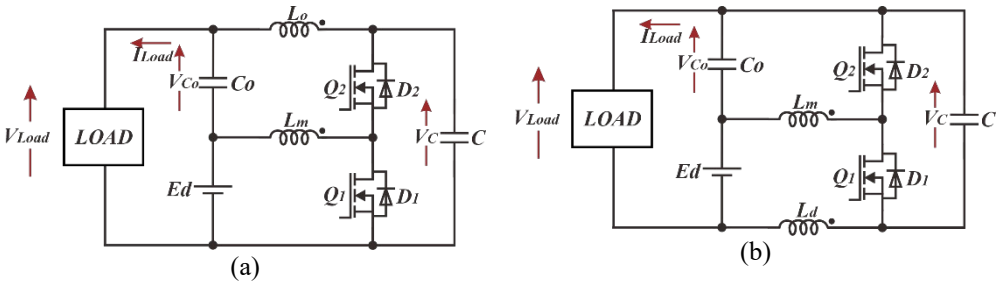


Fig. 4. Modified Cuk Converter Variations (a) Inductor Above, (b) Inductor Below

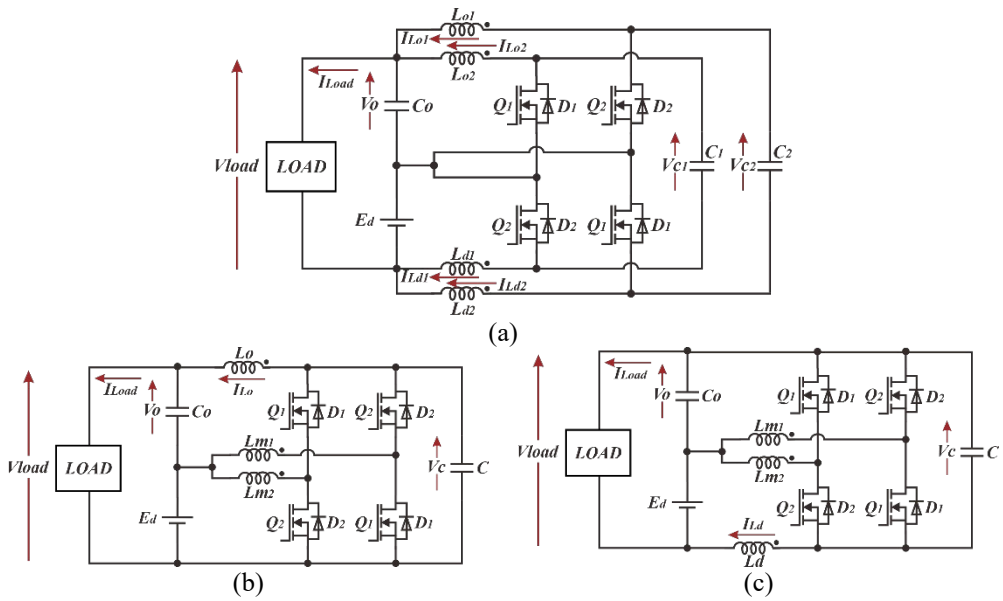


Fig. 5. Multiphase Modified Cuk Converter Variations (a) Top-Bottom Inductor, (b) Top-Middle Inductor, (c) Center-Bottom Inductor

The proposed multiphase topology in the modified Cuk converter can be developed into N-phase. Fig. 5 shows the circuit in the case of number of phases are two (N=2). Consequently, the number of components in the converter has doubled[20].

By using the same principle, the voltage expression can be derived for circuit shown in Fig. 5(a)-5(c), as shown in Eq. (7)-(9), respectively.

$$V_L = \frac{E_d}{1-\alpha} - \frac{V_Q}{1-\alpha} - \frac{NR_d(1-2\alpha+2\alpha^2) + R_Q\alpha + R_D(1-\alpha)}{N(1-\alpha)^2} I_{Ld} \quad (7)$$

$$V_L = \frac{E_d}{1-\alpha} - \frac{V_Q}{1-\alpha} - \frac{R_m + R_o N(1-\alpha)^2 + R_Q\alpha + R_D(1-\alpha)}{N(1-\alpha)^2} I_{Lo} \quad (8)$$

$$V_L = \frac{E_d}{1-\alpha} - \frac{V_Q}{1-\alpha} - \frac{NR_m\alpha^2 + R_d + R_Q\alpha + R_D(1-\alpha)}{N(1-\alpha)^2} I_{Ld} \quad (9)$$

By increasing the number of N-phases, it is possible to lower the voltage losses on transistors and inductors, as shown by Eq. (7)-(9). The voltage drop will decrease significantly as the number of phases, N, increases. The circuit topology of Fig. 5(b) has a smaller voltage drop due to the inductor than the circuit topology of Fig. 5(c), according to the Eq. (7)-(9). The reason for this is that the current flows in inductor Lo is lower than the inductor Ld's current flow. Additionally, it is evident that the voltage drops in the circuit shown in Fig. 5(c) are the highest because there are more components estimated and the result is notisltiplied by the duty cycle value. Of course, circuit topology of Fig. 5.(a) has the most components when considered from that perspective.

D. Multilevel-Multiphase Modified Cuk Converter

Given its advantages, the modified Cuk converter is also well-suited to serve as the based cell in the proposed multilevel topology. To extend the idea of maintaining low current ripple while obtaining higher voltage ratio, multiphase topology will be employed in the first level. The duty cycle that is employed at each level can vary thanks to the independent switch control that the proposed converter offers at each level. Fig. 6 [20] depicts the proposed multilevel multiphase modified Cuk circuit.

Ratio of the voltage of the proposed converter in Fig. 6 will exceed that of a single modified Cuk converter. This is because the second level's input voltage is derived from the first level's output capacitor voltage, and the third level's input voltage is then derived from the second level's output capacitor voltage. In addition, the fourth level's input voltage will be the third level's output capacitor voltage. As a result, the capacitor voltages at the first through fourth levels contribute to the overall voltage at the load.

Multiphase topology is employed on the proposed topology at the first level. The goal of this is to reduce the current ripple on the first level's input and output sides. Consequently, the subsequent level current ripple will be smaller compared to multilevel topology only without employing multiphase topologies. The fact that the third level's current flow is greater than the fourth level's is another factor if the multiphase topology is adopted in the second level. It will be important to keep in mind that a large ripple combined with a large current could be a significant issue. Thus, the first level's adoption of multiphase topology makes sense and can achieve the research objective, which is to provide a lower current ripple value.

3. Proposed Converter Analysis

A. Open Loop System Analysis

The topology described in Fig. 6 is scalable and can be modified to include more layers. The voltage equations for the converter shown in Fig. 6 are described in Eqs. (10)-(13). Eq. (10) represents the output capacitor voltage at the first level, which is used as the input for the second level. Similarly, Eq. (11) explains the output capacitor voltage at the second level, which serves as the input for the third level. Eq. (12) represents the output capacitor voltage at the third level, which serves as the input for the fourth level, as described in Eq. (13).

$$V_{o1} = E_d \frac{\alpha_1}{1-\alpha_1} - \frac{V_Q}{1-\alpha_1} - \frac{R_m + 2R_o(1-\alpha_1)^2 + R_Q\alpha_1 + R_D(1-\alpha_1)}{2(1-\alpha_1)^2} I_{Lo1} \tag{10}$$

$$V_{o2} = V_{o1} \frac{\alpha_2}{1-\alpha_2} - \frac{V_Q}{1-\alpha_2} - \frac{R_d(1-2\alpha_2+2\alpha_2{}^2) + R_Q\alpha_2 + R_Q(1-\alpha_2)}{(1-\alpha_2)^2} I_{Ld2} \tag{11}$$

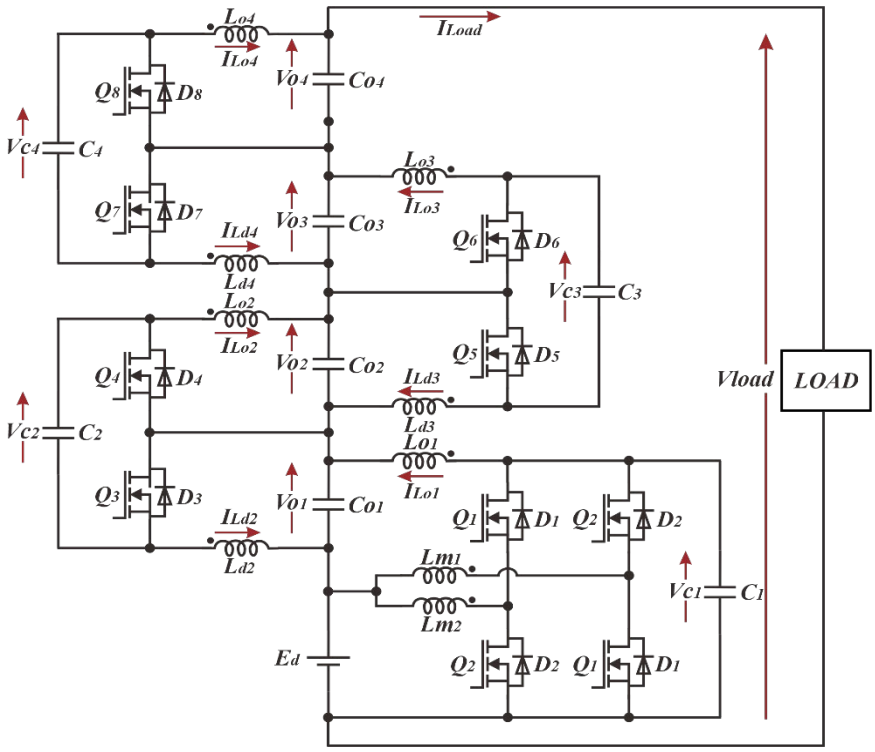


Fig. 6. Multilevel-Multiphase Modified Cuk Converter

$$V_{o3} = V_{o2}\frac{\alpha_3}{1-\alpha_3} - \frac{V_Q}{1-\alpha_3} - \frac{R_d(1-2\alpha_3+2{\alpha_3}^2)+R_Q\alpha_3+R_Q(1-\alpha_3)}{(1-\alpha_3)^2}I_{Ld3} \tag{12}$$

$$V_{o4} = V_{o3}\frac{\alpha_4}{1-\alpha_4} - \frac{V_Q}{1-\alpha_4} - \frac{R_d(1-2\alpha_4+2{\alpha_4}^2)+R_Q\alpha_4+R_Q(1-\alpha_4)}{(1-\alpha_4)^2}I_{Ld4} \tag{13}$$

Based on Eq. (10)-(13), the terminal voltage equation or the total voltage of the circuit is the sum of all voltage built up in each level, it will be obtained with the expression shown in Eq. (14). Eq. (15) shows the complete expression of output voltage.

$$\bar{v}_L = E_d + V_{o1} + V_{o2} + V_{o3} + V_{o4} \tag{14}$$

$$\begin{aligned}\bar{v}_L = E_d\Bigg[1 &+ \frac{\alpha_1}{1-\alpha_1} + \frac{\alpha_1\alpha_2}{(1-\alpha_1)(1-\alpha_2)} + \frac{\alpha_1\alpha_2\alpha_3}{(1-\alpha_1)(1-\alpha_2)(1-\alpha_3)} \\ &+ \frac{\alpha_1\alpha_2\alpha_3\alpha_4}{(1-\alpha_1)(1-\alpha_2)(1-\alpha_3)(1-\alpha_4)}\Bigg] \\ &- \Bigg[\frac{V_Q}{1-\alpha_1}\Big(1 + \frac{\alpha_2}{1-\alpha_2} + \frac{\alpha_2\alpha_3}{(1-\alpha_2)(1-\alpha_3)} \\ &+ \frac{\alpha_2\alpha_3\alpha_4}{(1-\alpha_2)(1-\alpha_3)(1-\alpha_4)}\Big)\Bigg] \\ &- \Bigg[\frac{V_Q}{1-\alpha_2}\Big(1 + \frac{\alpha_3}{1-\alpha_3} + \frac{\alpha_2\alpha_4}{(1-\alpha_2)(1-\alpha_4)}\Big)\Bigg] - \Bigg[\frac{V_Q}{1-\alpha_3}\Big(1 + \frac{\alpha_4}{1-\alpha_4}\Big)\Bigg] \\ &- \Bigg[\frac{V_Q}{1-\alpha_4}\Bigg] \\ &- \Bigg[\frac{R_d + R_o 2(1-\alpha_1)^2 + R_Q\alpha_1 + R_D(1-\alpha_1)}{2(1-\alpha_1)^2}I_{Lo1}\Big(1 + \frac{\alpha_2}{1-\alpha_2} \\ &+ \frac{\alpha_2\alpha_3}{(1-\alpha_2)(1-\alpha_3)} + \frac{\alpha_2\alpha_3\alpha_4}{(1-\alpha_2)(1-\alpha_3)(1-\alpha_4)}\Big)\Bigg] \\ &- \Bigg[\frac{R_d(1-2\alpha_2+2{\alpha_2}^2)+R_Q\alpha_2+R_Q(1-\alpha_2)}{(1-\alpha_2)^2}I_{Ld2}\Big(1 + \frac{\alpha_3}{1-\alpha_3} \\ &+ \frac{\alpha_2\alpha_4}{(1-\alpha_2)(1-\alpha_4)}\Big)\Bigg] \\ &- \Bigg[\frac{R_d(1-2\alpha_3+2{\alpha_3}^2)+R_Q\alpha_3+R_Q(1-\alpha_3)}{(1-\alpha_3)^2}I_{Ld3}\Big(1 + \frac{\alpha_4}{1-\alpha_4}\Big)\Bigg] \\ &- \Bigg[\frac{R_d(1-2\alpha_4+2{\alpha_4}^2)+R_Q\alpha_4+R_Q(1-\alpha_4)}{(1-\alpha_4)^2}I_{Ld4}\Bigg]\end{aligned} \tag{15}$$

Non-idealities of transistors and inductors make up the parasitic components in Eq. (15). In an ideal circumstance, it would be possible to omit the parasitic components and simplify Eq. (15) as in Eq. (16).

$$\begin{aligned}\bar{v}_L = E_d\Bigg[1 &+ \frac{\alpha_1}{1-\alpha_1} + \frac{\alpha_1\alpha_2}{(1-\alpha_1)(1-\alpha_2)} + \frac{\alpha_1\alpha_2\alpha_3}{(1-\alpha_1)(1-\alpha_2)(1-\alpha_3)} \\ &+ \frac{\alpha_1\alpha_2\alpha_3\alpha_4}{(1-\alpha_1)(1-\alpha_2)(1-\alpha_3)(1-\alpha_4)}\Bigg]\end{aligned} \tag{16}$$

If a duty cycle value of 0.5 is used in Eq. (16), the voltage gain will equal to (N+1) times of the source voltage (Ed). This is an important characteristic of the multilevel topology, which exhibits modularity and self-balancing resulted at the same output voltage for every cell. Under this situation, the voltage for every level can be expressed generally as shown in Eq. (17).

$$\bar{v}_L n\ level = E_d\Big[1 + n\frac{\alpha}{1-\alpha}\Big] \tag{17}$$

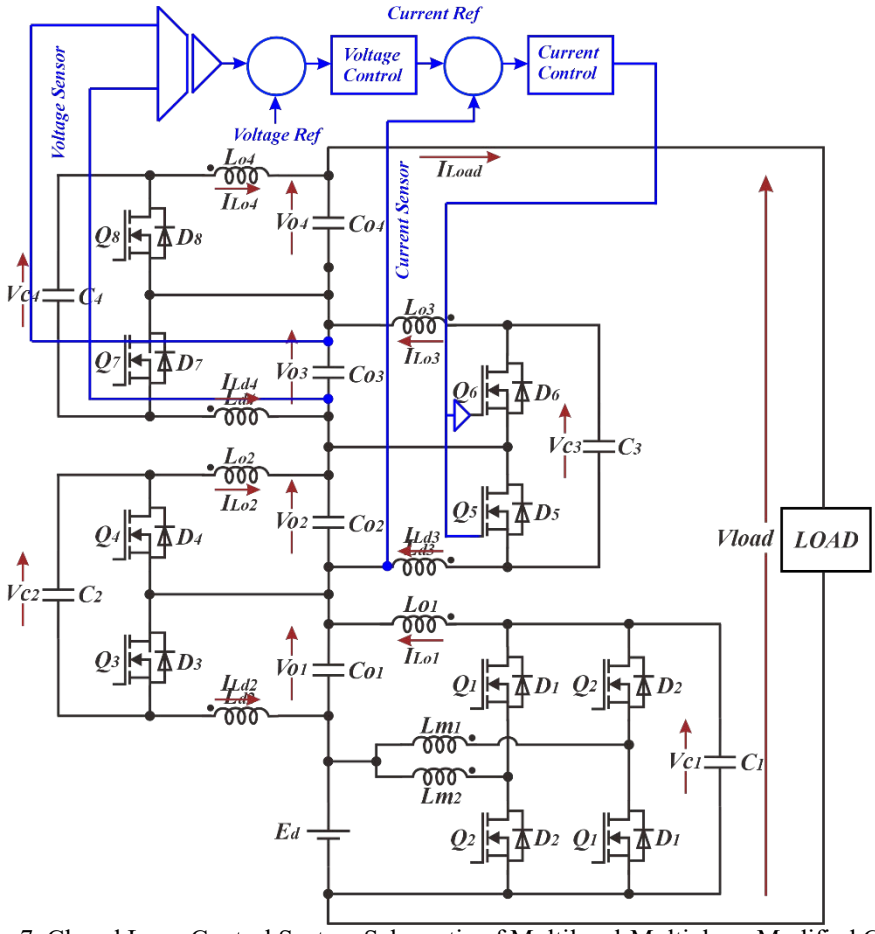


Fig. 7. Closed Loop Control System Schematic of Multilevel-Multiphase Modified Cuk Converter

B. Closed Loop System Analysis

The circuit depicted in Fig. 6 will be integrated into a closed-loop control system, where the third cell will be subject to both voltage and current control. This approach is necessary to reduce Current ripple on both the input and output sides. using a multiphase technique. To achieve this, the duty cycle values of the first and fourth cells must remain constant. During an open-loop control system experiment, the ideal duty cycle value was determined to reach the target output voltage of 380-to-400 VDC. Within a closed-loop control system, the duty cycle of the third cell can be safely adjusted within a broad range of 0.55 to 0.75. Fig. 7 illustrates the schematic of the proposed closed-loop control system.

The proposed closed-loop control system utilizes a double-loop control strategy based on a proportional-integral (PI) controller scheme. In this configuration, the outer voltage control loop is designed with a smaller bandwidth than the inner current control loop, indicating that the voltage control response time will be slower than that of the current control . Fig. 8 shows the schematic of the proposed double-loop closed-loop control system.

The operation in continuous mode has been analyzed and modeled using state-space equations for the circuit depicted in Fig. 3. The state-space equation for the condition when Q1 is ON is derived by applying a duty cycle equal to D, while for the condition when Q2 is ON, the duty cycle is 1-D. The state-space equations for the modified Cuk converter in each condition are expressed in Eqs. (18)-(19) .

$$\dot{X} = A_{on}X + B_{on}Y \tag{18}$$

$$\dot{X} = [DA_{on} + (1-D)A_{off}]X + [DB_{on} + (1-D)B_{off}]Y \quad (19)$$

If Eq. (19) is modeled based on small-signal linearization, the duty cycle D is denoted by d, then Eq. (20) can be obtained.

$$\dot{x} = Ax + Fd \quad (20)$$

Eq. (20) then transformed by using Laplace transformation to obtain the representation in the frequency domain as shown by Eq. (21).

$$\frac{x\,(s)}{d\,(s)} = [sI - A]^{-1}F \quad (21)$$

As a result, the state-space averaging outcomes will be derived in Eqs. (22)-(23) when used on the modified Cuk converter with the provided parameters.

$$\left[\frac{I_d\,(s)}{d\,(s)}\right] = \left[\frac{CC_oL_oV_cs^3 - C_oL_o(I_d+I_o)(-1+D)s^2 + V_c(C_oD+C)s - (I_d+I_o)(-1+D)}{CC_oL_dL_os^4 + \left(((L_d+L_o)D^2 - 2DL_o + L_o)C_o + CL_d\right)s^2 + (-1+D)^2}\right] \quad (22)$$

$$\left[\frac{V_o\,(s)}{d\,(s)}\right] = \left[\frac{CL_dV_cs^2 - L_dD(I_d+I_o)s - V_c(-1+D)}{CC_oL_oV_cs^3 - C_oL_o(I_d+I_o)(-1+D)s^2 + V_c(C_oD+C)s - (I_d+I_o)(-1+D)}\right] \quad (23)$$

The circuit's current is regulated by the inner loop's closed-loop control system, as illustrated in Fig. 8. In this system, the reference current value provided by the outer loop control is compared to the measured current in the inductor at the third level of the proposed topology. To determine the value of Tp1(s), the component parameter values will be calculated using Eq. (16). The inner loop's current control must respond more quickly than the outer loop's voltage control. Consequently, the measurement value and inductor current compensation must deliver faster responses. The current control method in the inner loop, as depicted in Fig. 9(a), is described by the expression in Eq. (24).

$$T_{OL1}(s) = T_{c1}(s) \cdot T_{p1}(s) \cdot H(s) \cdot T_m(s) \quad (24)$$

Current sensor of IL has the transfer function, H(s), assumed to be 100% accurate so that it has unity gain. Tm(s) represents the circuit's modulator transfer function. The PI control block, Tc1(s), is described by Eq. (25).

$$T_{c1}(s) = K_p\frac{K_i}{s} \quad (25)$$

In a circuit control system, the outer loop regulates the voltage. The reference voltage value is compared to the observed output voltage at the third level. To calculate the value of Tp2(s), the component parameters' values will be determined using Eq. (21). Eq. (26) expresses the equation that represents the strategy of the outer voltage control loop, as shown in Fig. 9b.

$$T_{OL2}(s) = T_{c2}(s) \cdot T_{p2}(s) \cdot H(s) \quad (26)$$

The voltage sensor of Vc has the transfer function, H(s), assumed to be 100% accurate so that it has unity gain. The PI control block, Tc2(s), is described using Eq. (27).

$$T_{c2}(s) = K_p\frac{K_i}{s} \quad (27)$$

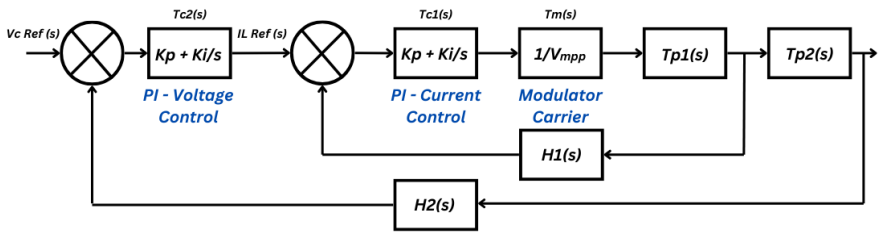
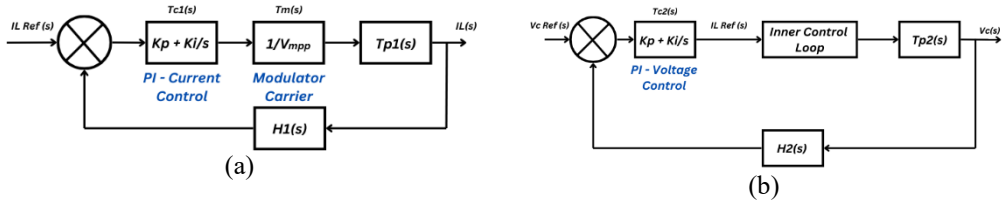
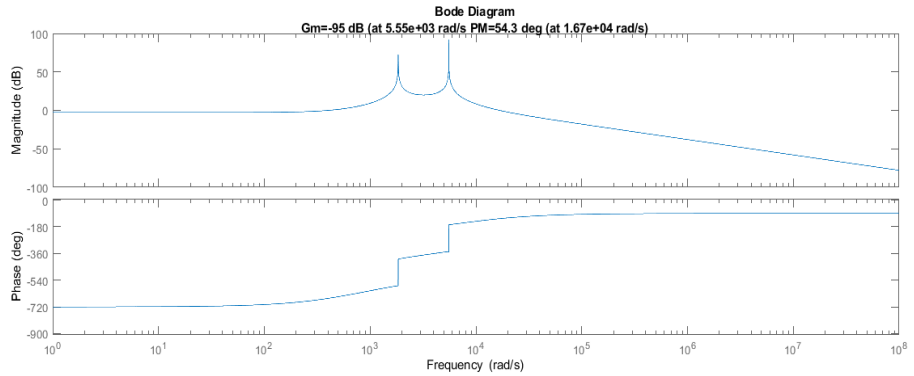


Fig. 8. Schematic of the Double-Loop Closed-Loop Control System

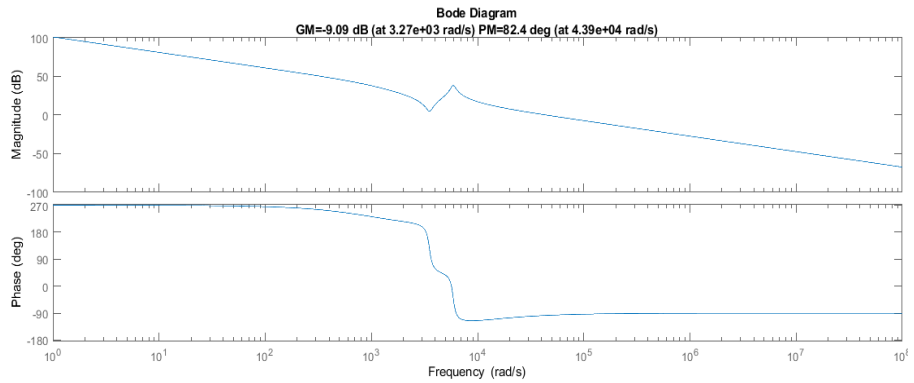


(a) (b)

Fig. 9. Control System Schematic: (a) Inner Loop Current, (b) Outer Loop Voltage



(a)



(b)

Fig. 10. Bode Plot: (a) Current Control, (b) Voltage Control

The PI (Proportional-Integral) values for this includes both current and voltage controls study are then calculated and derived. The PI values obtained in current control are Ti = 1.0419e-4, Ki = 9017.6304, and Kp = 0.9395. The PI values found for voltage control are Ti = 3.1283e-3, Ki = 169.2876, and Kp = 0.0529. Fig. 10 shows the generated Bode plot for each control. The proposed control is stable.

4. Verification of Results and Analysis

A. Open Loop System Results and Analysis

A.1. Simulation and Experiment Results

The circuit shown in Fig. 6 will be utilized in the open-loop experiment. Fig. 11 illustrates the circuit configuration for this experiment. An example of the experimental setup is provided in Fig. 12. The parameters employed in the experiments are listed in Table 1.

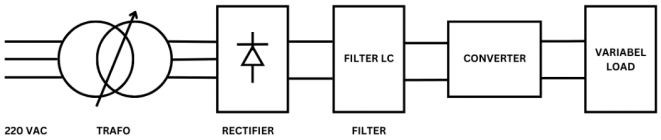


Fig. 11. Schematic of the Experiment

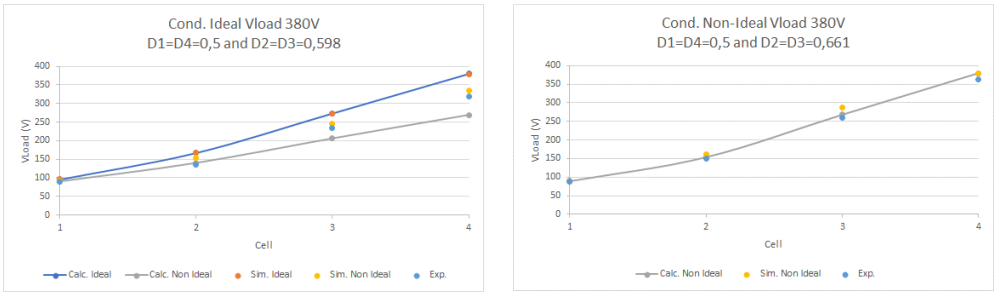
Fig. 12. Photos of the Experimental Equipment in the Laboratory

Table 1. Experimental Component Parameters

Parameters	Value
Power Capacity	600 – 1000 W (800 W)
Inductor	2 mH, Sendust
Capacitors	22 µF, JFX Film
Ripple Current	1,3 A (Max)
Switching	IGBT MagnaChip 60T65PES
Frequency Switching	20 kHz

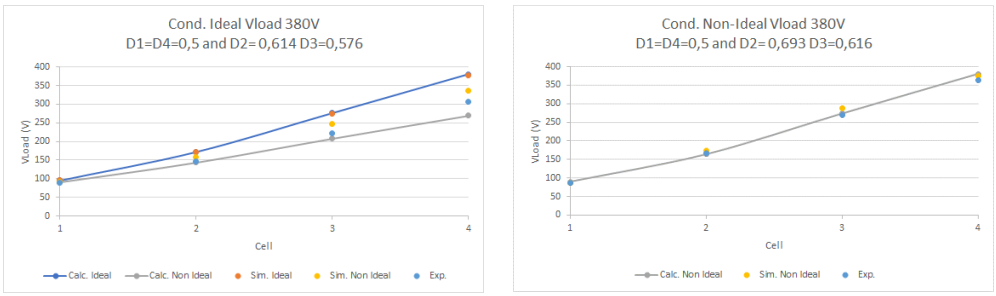
This research employs a multilevel, multiphase modified DC-DC Cuk converter designed to meet the voltage requirements of a DC microgrid, specifically targeting an output voltage of 380–400 VDC. This output voltage is achieved by boosting the source voltage from a PV system or battery from 48 VDC. The output voltage equations under non-ideal and ideal conditions are represented by Eq. (15) and Eq. (16), respectively, and are used to calculate the duty cycle value and output voltage. Prior to simulation, these calculations are performed using Microsoft Excel's Solver tool to determine the correct duty cycle value. The calculation and simulation results are depicted in Fig. (13)-(16).

Figures (13)-(16) illustrate significant differences between voltages in ideal and non-ideal scenarios. These differences arise because, in ideal calculations, parasitic components are not considered, leading to a lower duty cycle value compared to non-ideal circumstances. The second-level voltage will reflect voltage differential at the first level, further amplifying the discrepancy. Consequently, the voltage differential between the third and fourth levels' output voltages will rise. Experimental tests will later confirm the simulation and calculation results. These experimental outcomes will be compared with the previously conducted calculations, simulations, and experimental. The results are also presented in Figures (13)-(16).



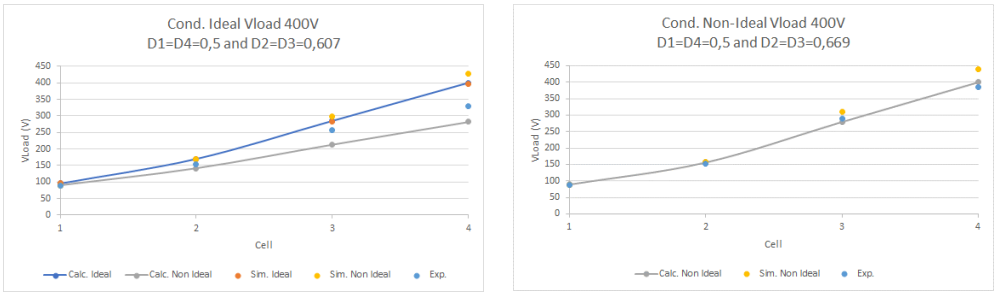
(a) (b)

Fig. 13. Calculation, Simulation, and Experiment of Output Voltage 380V D2=D3
(a) Ideal, (b) Non-Ideal



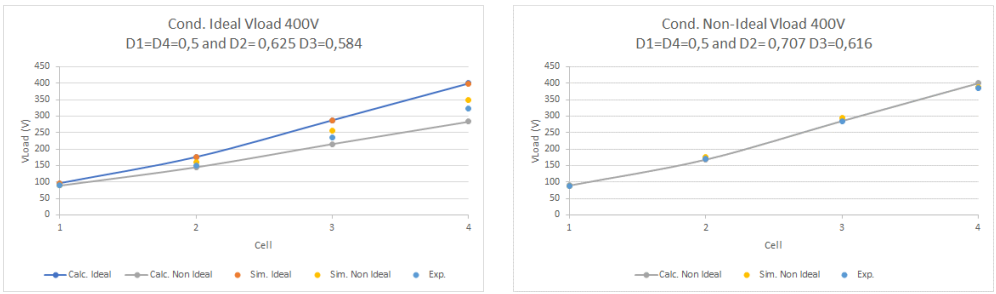
(a) (b)

Fig. 14. Calculation, Simulation, and Experiment of Output Voltage 380V D2≠D3
(a) Ideal, (b) Non-Ideal



(a) (b)

Fig. 15. Calculation, Simulation, and Experiment of 400V Output Voltage D2=D3
(a) Ideal, (b) Non-Ideal



(a) (b)

Fig. 16. Calculation, Simulation, and Experiment of 400V Output Voltage D2≠D3
(a) Ideal, (b) Non-Ideal

It was discovered that the values acquired from non-ideal experimental findings are much closer to the experimental outcomes than the ideal conditions. This is because non-ideal calculations account for the parasitic components present in each circuit, resulting in results that are more in line with the experimental setup's inherent non-ideality. The experimental results of the open-loop control system revealed that the duty cycle values appropriate as references for the closed-loop control system were derived under non-ideal situations. Specifically, the duty cycle values are $\alpha1=\alpha2=0.5$, $\alpha3=0.707$, and $\alpha4=0.616$.

A.2. Current Ripple

In this experiment, the current ripple on both the input and output sides was observed. The primary objective of using a multiphase topology is to minimize the current ripple. The current ripple on the input side and output side was recorded and is presented in Fig. 17 and Fig. 18.

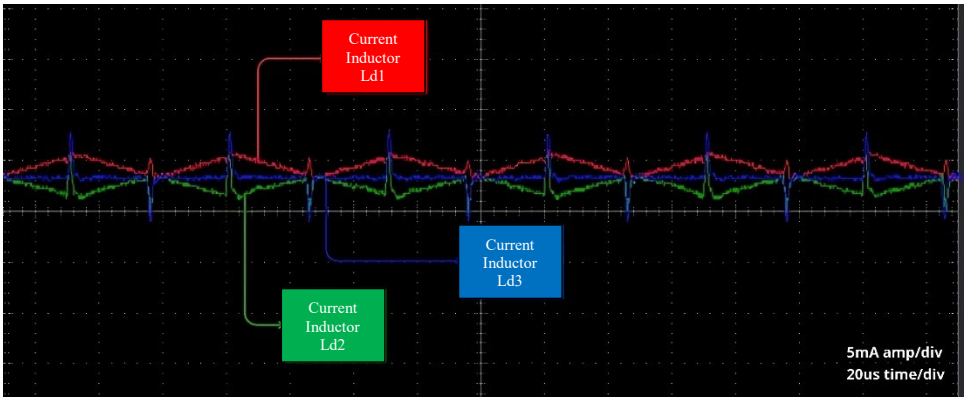


Fig. 17. Input Side Current Ripple

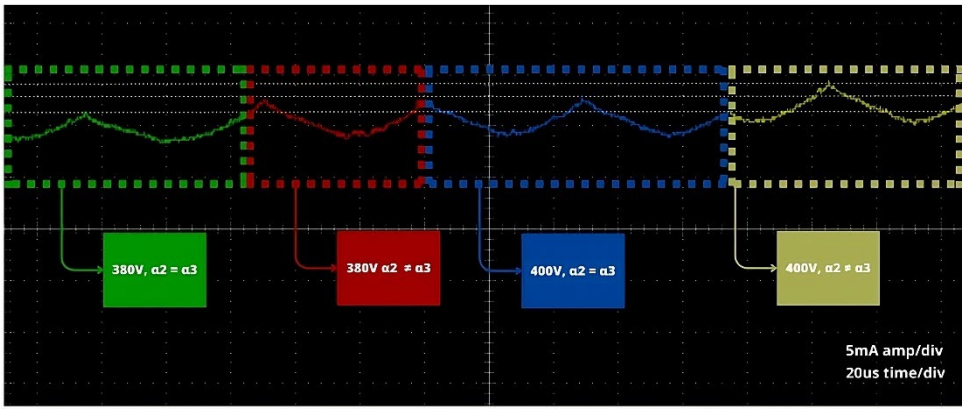


Fig. 18. Output Side Current Ripple

Fig. 17 illustrates how the application of multiphase topology causes ripple cancellation to occur in the current ripple generated on the input side. This matches the goal of employing multiphase topology, which is to reduce current ripples, the result is the input side's current ripple to be extremely small and generates constant current. Fig. 18 shows the output side current ripple for every duty cycle experiment. The graphic illustrates the observed output current ripple is very small. The duty cycle value in the circuit undoubtedly has an influence on this situation. Although the fourth cell is kept at a duty cycle of 0.5 in the attempt of suppressing the output current ripple, the second and third cells do not suppress the ripple, so it is observed that the output current ripple remains. The ripple current value increases with increasing duty cycle value.

A.3. Power Loss Fraction and Efficiency

Typically, power converter is susceptible to three different kinds of power losses: losses of inductor, conduction, and switching. The inductor losses are due to the characteristics of iron core, DC resistance, and AC resistance. While in the switching device the DC resistance and internal voltage drop across each transistor or diode make up the conduction and switching losses. In this proposed topology, the loss fraction is determined by the loss analysis. Operating conditions of the circuit are used for this analysis in non-ideal condition. The non-ideal condition equation includes parasitic components. The gain fraction's computation results are shown in Fig. 19.

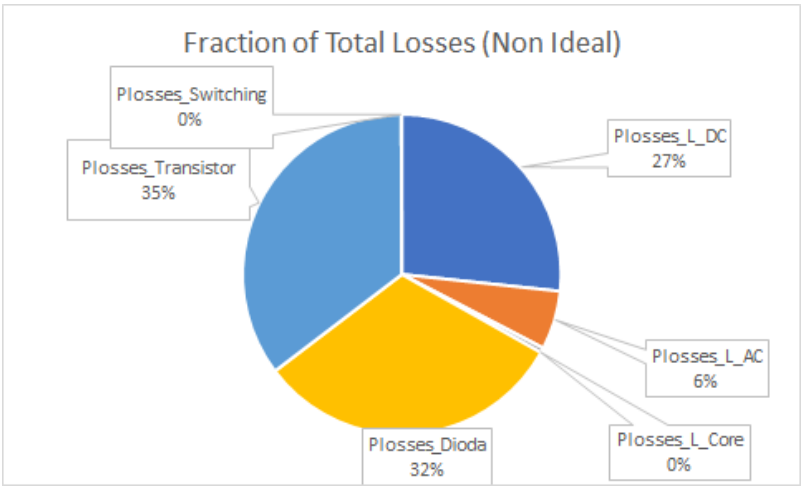


Fig. 19. Non-Ideal State Circuit Power Loss Fraction

Fig. 19 illustrates the distribution of losses in the proposed converter, showing that they are predominantly due to the switching component, which accounts for nearly 67% of the total power loss, and the inductor component, which contributes almost 33%. The overall power losses amounted to 180 W. This study aims to reduce power losses. It is recommended to use a switching device with higher specifications, such as SiC (Silicon Carbide) or GaN (Gallium Nitride), instead of the conventional devices used in the experiment.

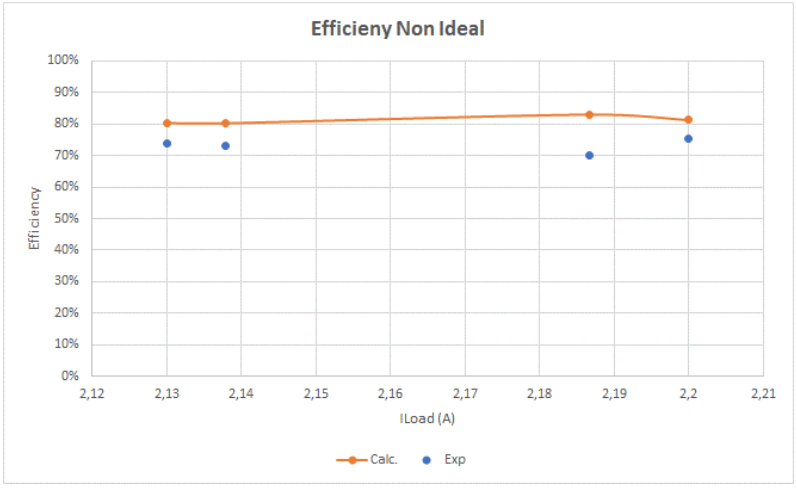


Fig. 20. Non-Ideal State Circuit Efficiency

By utilizing the data obtained from both calculations and experimental power measurements, the efficiency of the proposed converter is confirmed. This circuit operates with a total power range of 700–1000 W. During the experiments, the duty cycle was varied to gather data under non-ideal conditions. The efficiency of the proposed converter is depicted in Fig. 20.

The proposed converter circuit exhibits an efficiency exceeding 70% in the conducted experiments, as shown in Fig. 20. There is a small 7% to 10% discrepancy between the calculated and experimental results. This shows that the conducted losses analysis and calculation results describe the circuit's actual conditions. The experiment confirms the losses analysis, therefore the performed analysis can serve as a guide for improving the efficiency.

B. Closed Loop System Results and Analysis

B.1. Simulation Results

To observe the dynamic behavior of the proposed converter under closed-loop control system, simulations by PSIM are carried out. The resulting data will be processed by MATLAB to provide the graph visualization. This simulation uses two types of variations: variation of reference voltage and variation of source voltage. Fig. 21 and Fig. 22 show the simulation results for two different cases, respectively.

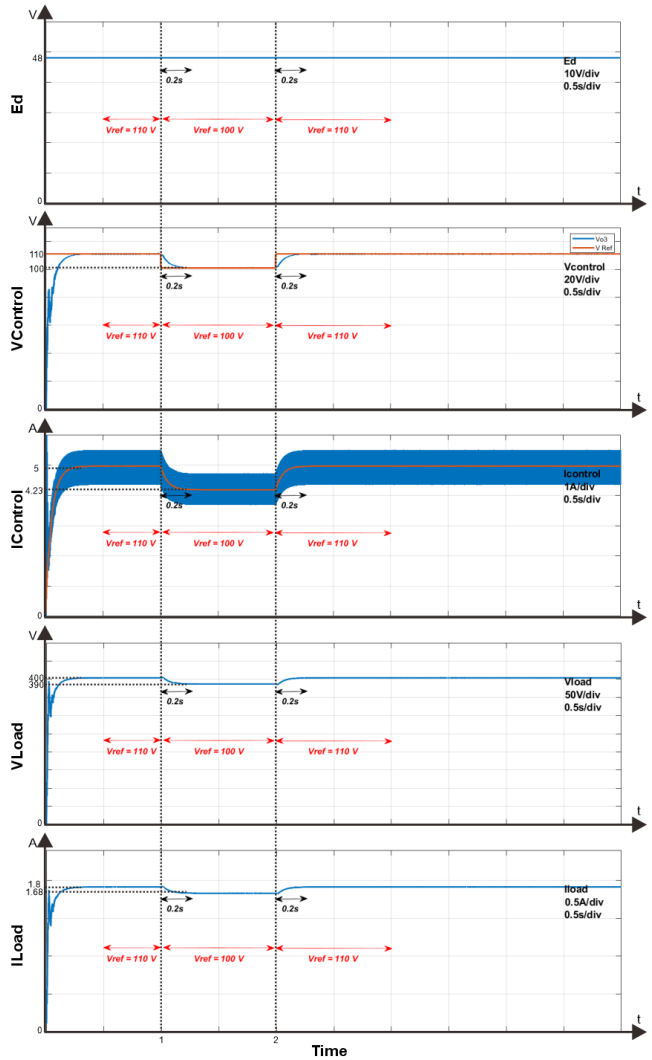


Fig. 21. Simulation Results of Variation Voltage Variation

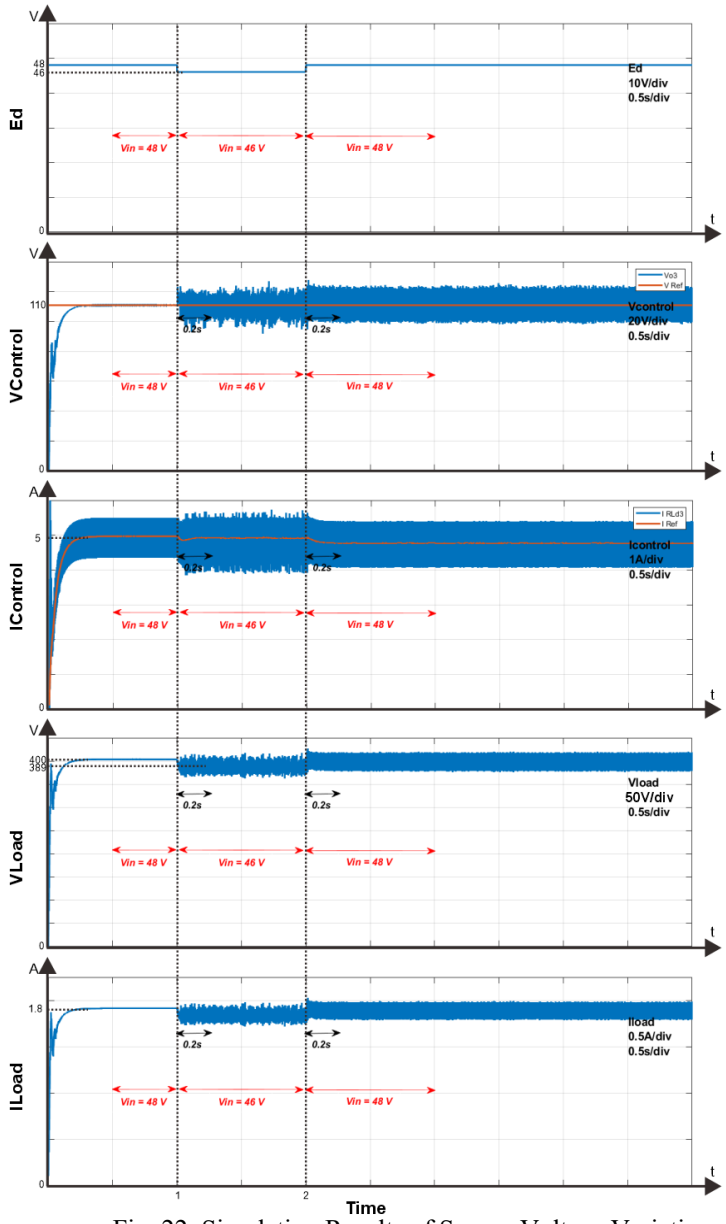


Fig. 22. Simulation Results of Source Voltage Variation

The simulation presented in Fig. 21 was executed with one-second intervals. Initially, the reference voltage was reduced by 10 V, from 110 V to 100 V, during the first second. At the two-second mark, the reference voltage was restored to 110 V. The designed control system demonstrated its capability to track these reference voltage changes within 0.2 seconds. Similarly, the simulation depicted in Fig. 22 was conducted with one-second intervals. During the first second, the source voltage decreased by 2 V, from 48 V to 46 V. At the two-second mark, the source voltage was restored to 48 V. The control system efficiently maintained the voltage at the reference level, even under source voltage perturbations.

B.2.Experiment Results

The proposed converter circuit depicted in Fig. 7 is the one used for the closed-loop experiment. The experimental setup for the closed-loop control is shown in Fig. 23. The experimental parameters utilized in the study are listed in Table 2.

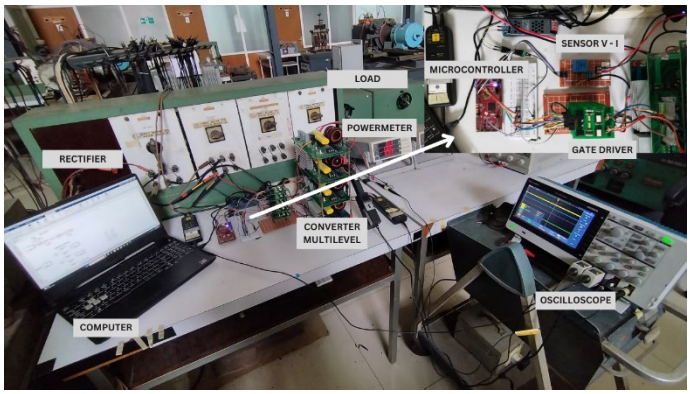


Fig. 23. Photos of the Experimental Equipment in the Laboratory

Table 2. Experimental Component Parameters

Parameters	Value
Power Capacity	600 – 1000 W (800 W)
Inductor	2 mH, Sendust
Capacitors	22 µF, JFX Film
Ripple Current	1,3 A (Max)
Switching	IGBT MagnaChip 60T65PES
Frequency Switching	20 kHz
Voltage Vco3	110 V
Current ILd3	5 A
Reference Voltage	110 V

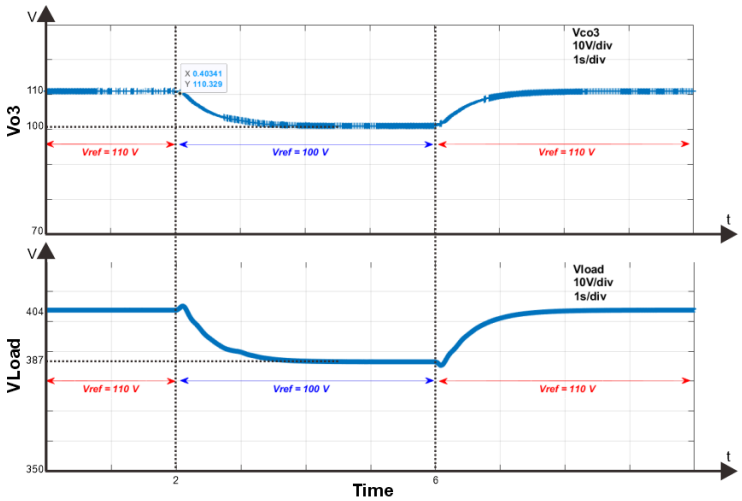


Fig. 24. Experiment Results of Reference Voltage Variation (a) Vco3, (b) Vload

In this experiment, data was collected only for the reference voltage variation. The experimental results are presented in Fig. 24, which shows the performance of the proposed converter under varying reference voltages. Fig. 24 displays the experiment results for the third-level cell voltage and the total load voltage. The experiment was conducted in 4-second intervals, starting with an initial reference voltage of 110V. At the 2-second mark, the reference voltage was reduced by 10V to 100V, and then at 5 seconds, it was increased back by 10V to 110V, returning to the initial reference value. The designed control system effectively tracks the reference voltage, with the system responding to changes in less than 1.5 seconds. The control system demonstrates accurate, fast, and responsive adaptation to the reference voltage variations.

5. Conclusion

A multilevel multiphase topology based on modified DC-DC Cuk converter has been proposed in this research paper. The four levels converter that is generated can provide a high ratio of input to output voltage while maintaining lower current ripple in the input and output sides. The first level will process the input voltage, can be either from photovoltaic panel or battery, to be the input for the second level, subsequently until the fourth level to achieve a high ratio output voltage. The proposed converter can achieve the output voltage of 380-400 VDC from 48 VDC input voltage with a relatively moderate duty cycle, $\alpha1=\alpha2=0.5$, $\alpha3=0.707$, and $\alpha4=0.616$, under non-ideal converter conditions.

The derived equations for the proposed converter have also been given by showing the voltage reduction equations caused by component resistance and switch drop voltage. Calculations, simulations, and experiments on the open-loop control system have also been given. From the open circuit system condition, the current ripple of each level has also been shown to prove that the multiphase topology of the first level has a great impact on the subsequent levels. The fractional analysis of the power loss in the proposed converter has been conducted to assess its efficiency. The efficiency of the proposed converter has been determined to be in the range of 70% to 80%.

The closed-loop control system, consisting of the outer voltage control loop and the inner current control loop, has been implemented. Stability analysis based on Bode Plot has been confirmed. The experiment results show that the proposed converter equipped with the proposed control scheme can track changes and achieve desired operation point under various conditions.

6. Acknowledgment

The authors would like to express their gratitude to the late Prof. Pekik Argo Dahono, whose devotion and example continue to inspire, even though he is no longer with us. His dedication to the students he served during his career has left a lasting impression.

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