Performance Evaluation and Control Technique of Large Ratio DC-DC Converter

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Abstract: The performance of large ratio dc-dc converter will be discussed in this paper. The performance will be observed by its ripple and losses. The performance will be compared with multiphase and multilevel dc-dc converter. The specific control technique for large ratio dc-dc converter also will be discussed in this paper. Experiment results are included to verify the analysis method.

Keywords: Ripple, losses, control.

1. Introduction

RENEWABLE energy power generations such as photovoltaic, fuel cell, and others dc output voltage power generation, are very promising due to the environmental consideration and limited fossil fuel. This renewable energy, especially solar energy is very potential in Indonesia. This is very useful to electrify remote area in Indonesia.

However, the output voltage of the photovoltaic cell is very low, around 6V-24V. Therefore, the output voltage cannot be directly to be used. The output voltage must be stepped up and inverted to produce appropriate ac voltage.

In case of step down, there are some applications that need a very low dc voltage from grid, such as microprocessor, electroplating, etc. To gather the very low voltage, grid line must be rectified and stepped down. Of course, the other option is to utilize transformer. But the physical size and cost is considerations to avoid transformer. Because of that, step down and step up processes are expected in dc voltage.

There are problems to step up and step down dc voltage to very high and very low dc voltage. In non-isolated dc-dc converter type, high ratio between input and output converter will create problem due to limitation of the switching device. High ratio between input and output will make the switching device operate in very small or very high duty ratio while as we know there are some limitations in the non-ideal switching device. To solve this problem, a new topology of dc-dc converter is proposed[2]. This topology let us obtain the high ratio of the input and output from the potential difference of the each converter. Thus we will not face the extreme duty cycle problem in the switching device anymore since we can operate each converter in the moderate duty cycle.

In this paper, performance of large ratio dc-dc converter will be observed from the ripple and losses aspects. Control technique of large ratio dc-dc converter also will be discussed. The control technique is utilizing double loop control.

2. Large Ratio Dc-Dc Converter

Suppose that we want to obtain large ratio buck dc-dc converter as mentioned before, then we consider the parallel-input, series output configuration (Fig. 1) of buck converter. Fig. 2(a) shows the two buck converters which will be connected in the configuration as shown in Fig. 3.

The load side is represented by a current source, while input side is represented by voltage source. Since input side of buck converter is connected in parallel, then

$$E_{d1} = E_{d2} = E_d \qquad (1)$$

Where E_{d1}, E_{d2}, and E_d are input voltage of first buck converter, second buck converter, and the new topology converter, respectively.

Connecting the input side of the two buck converters in parallel manner will result a circuit as shown in Fig. 2(b). Now the two converters have been connected into single converter with two outputs. Then we had to connect the two outputs in serial manner, since the both output currents are flow in the opposite direction, then we have to reverse one of the output current so it can be connected in serial manner. The reversal of the one of the output current can be done in the control domain of the buck converter. Fig. 2(c) shows the resulted topology after the reversal of another output

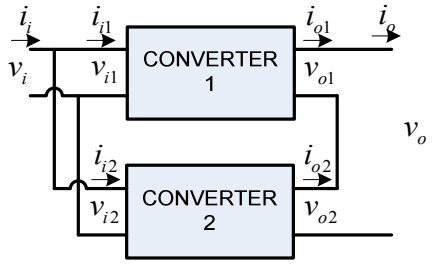


Fig. 1. Parallel – Input, Series – Output configuration.

current. Since two current sources which are connected in series are degenerated into a single current source, then Fig. 2(d) shows the resulted topology. The complete new topology large ratio dc-dc converter is shown in Fig. 2(e) where the transistors and diodes used as switching device. With this topology we can obtain large ratio between output and input side, without need to operate each switching device in the extreme duty cycle, as in the conventional buck converter.

Configuration as shown on Fig. 3 is the proposed large ratio dc-dc converter in the opposite direction of power flow, in the other word it is boost dc-dc converter, which also will be discussed later.

Lets us move to the control strategy of the proposed new topology large ratio buck dc-dc converter. As mentioned above the large ratio conversion in the output from the output can be done without operate the switching device in the extreme duty cycle. It can be done since by using the proposed new topology we can control each converter independently. To show the independently control, let us see Fig. 2(e) once again.

The voltage between node a and node n is the output of the first buck converter, so it can be expressed as

$$v_{an} = \begin{cases} 0 & \text{when } S_1 \text{ off} \\ E_d & \text{when } S_1 \text{ on} \end{cases} \qquad (2)$$

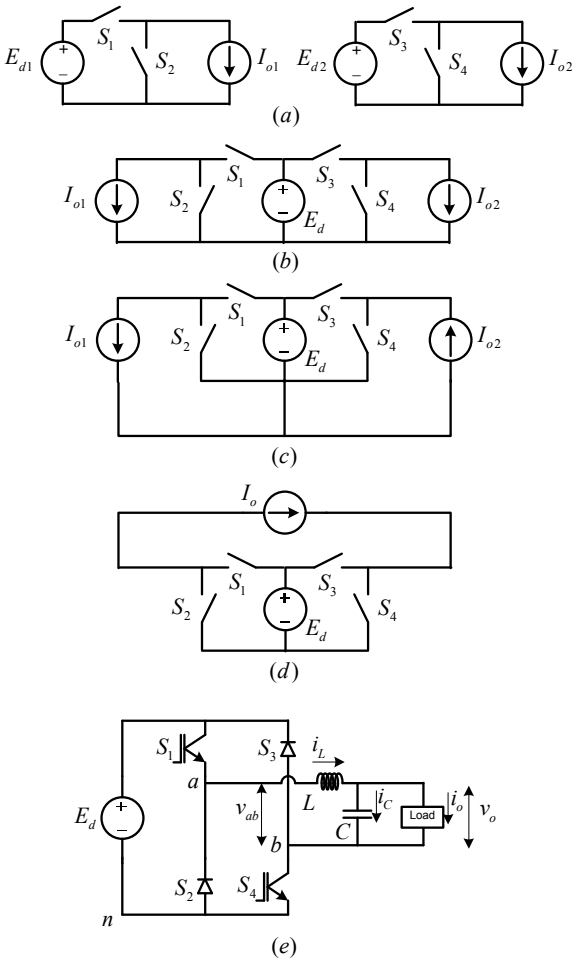


Fig. 2. Detail of the derivation of large ratio dc-dc converter.

If the duration of S_1 off and on is called T_{off1}, and T_{on1}, respectively, and a period of a consecutive T_{off} and T_{on} is called T_s, then the average value of v_{an} in a period of switching is expressed as:

$$v_{AN}T_s = 0.T_{off1} + E_d T_{on1} \tag{3}$$

Thus

$$v_{AN} = E_d \frac{T_{on1}}{T_s} = E_d D_1 \tag{4}$$

Where v_{AN} is the average value of v_{an}, and $D_1 = T_{on1}/T_s = v_{AN}/E_d$ is the duty cycle of the switches in the first buck converter. Using similar way, then we can obtain the average value of v_{bn}

$$v_{BN} = E_d \frac{T_{on2}}{T_s} = E_d D_2 \tag{5}$$

Where v_{BN} is the average value of v_{bn}, and $D_2 = T_{on2}/T_s = v_{BN}/E_d$ is duty cycle of the switches in the second buck converter. The load is connected across node a and b, so the load voltage can be expressed as

$$v_{load} = v_{AN} - v_{BN} \quad (6)$$

$$v_{load} = E_d D_1 - E_d D_2 \quad (7)$$

$$v_{load} = E_d \left(D_1 - D_2 \right) \quad (8)$$

From (8) is clearly shown that we can obtain small value of v_{load} if the (D_1-D_2) term is made small. Thus to obtain the small value of (D_1-D_2), we do not have to set
D_1 and D_2 in small value too, rather we can choose moderate value of D_1 and D_2 as long as the subtraction result is small. So we will get large ratio between output and input of this proposed converter, while the switching devices are operated in the moderate duty cycle. Thus we will have infinite combinations of D_1 and D_2 value which can be chosen to give small value of (D_1-D_2). But the combination of D_1 and D_2 around 0.5 will give the most optimum results, since with this value we will get minimum ripple in the input and output of the proposed converter compared to the other combinations of D_1 and D_2 values.

In the operation as boost converter, the topology derived using the same approach is shown in Fig. 3. Let us assume that voltage in the load is called v_C, then according to Fig. 3,

$$v_C = E_d + v_L + v_{S_3} + v_{S2} \quad (9)$$

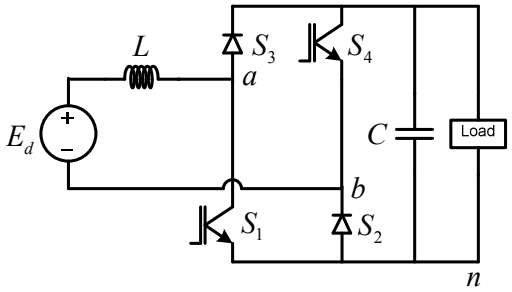


Fig. 3. Large ratio boost dc-dc converter

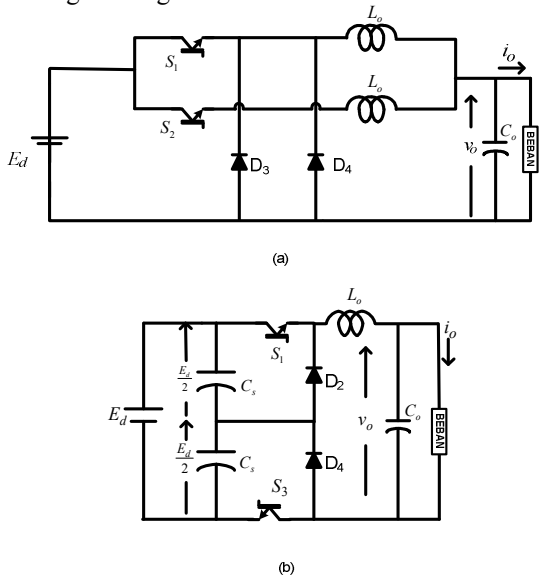


Fig. 4. (a) Two-phase, and (b) Three-level, dc-dc converter.

Where v_L, v_{S3}, v_{S2} are voltage across inductor, S_3, and S_2, respectively. v_{S2} itself can be expressed as

$$v_{S_2} = \begin{cases} 0 & \text{when } S_1 \text{ off} \\ v_C & \text{when } S_1 \text{ on} \end{cases} \quad (10)$$

Thus the average value of v_{S2} over one switching period is

$$v_{S_2,av} = k_1 v_c \quad (11)$$

Where $v_{S2,av}$ is the average value of v_{S2} and k_1 is the duty cycle of the switch S_1. Using the same way, the average value of voltage across S_3 can be expressed:

$$v_{S_3,av} = k_2 v_c \quad (12)$$

Where $v_{S3,av}$ is the average value of v_{S3} and k_2 is duty cycle of switch S_2. Since the average voltage across an inductor over one switching period is zero, then (9) can be expressed as

$$v_C = E_d + k_1 v_C + k_2 v_C \quad (13)$$

$$v_c = \frac{1}{1-(k_1+k_2)} E_d \quad (14)$$

Clearly shown in (14), if we want to obtain very big output voltage compare to its input voltage, then we should set the D or (k_1+k_2) term as near as unity. Thus we need not to set each k_1 and k_2 in the value near unity, as long the (k_1+k_2) is near unity. This is another interesting point of the proposed large ratio boost converter topology, we can obtain very high output voltage without need to operate the switches in extreme duty cycle. Examples for the application of this converter is to step up output voltage of renewable energy power generator, in order to transfer the electricity, such as photovoltaic cell, fuel cell, and others dc voltage power generator.

3. Performance of Large Ratio Dc-Dc Converter

The performances of large ratio dc-dc converter will be compared to existed dc-dc converters. They are multiphase and multilevel dc-dc converters. Large ratio dc-dc converters utilize four switches, therefore, this dc-dc converter will be compared with two-phases dc-dc converter and three-level dc-dc converter, as shown in Fig. 4. To simplify the analysis of large ratio dc-dc converter performances, buck converter will be considered in this analysis. This analysis is also valid for boost converter.

A. Ripple Analysis

At the input side of dc-dc converter, there is usually LC filter to minimize the input current ripple of converter. If dc-dc converter is utilized as power supply, then at the output side there should be another LC filter. Ripple analysis is needed to know the ripple existed at the input and output side of proposed large ratio dc-dc converter. This information is needed to determine the size of filter LC needed for the specified ripple. Commonly, ripple analysis is done with Fourier series concept. With this concept, accurate result will be obtained with all harmonics. However, this concept takes times.

Therefore, ripple analysis will be done with time domain approach. With this approach, accurate result also can be obtained without taking into account the harmonics[3].

Output Ripple Analysis

To analyze the output ripple, some assumptions will be taken into account. Voltage source is a non-ripple ideal voltage source, transistor switches and diodes are ideal switches. Capacitor filter is ideal capacitor without resistance. This analysis will be limited in continues conduction mode.

Output waveform details are shown in Fig. 6(b). v_{ab} is output voltage. $\tilde{i}_L$ and $\tilde{v}_o$ are the ripple current in inductor and voltage in capacitor respectively.

To analyze output ripple current, then the start point is stating the voltage a-b point as

$$v_{ab} = L\frac{di_L}{dt} + v_o \tag{15}$$

Current and voltage in Eq. (25) can be separated to average and ripple component as follows,

$$v_{ab} = \overline{v}_{ab} + \tilde{v}_{ab} \tag{16}$$

$$i_L = \overline{i}_L + \tilde{i}_L \tag{17}$$

$$v_o = \overline{v}_o + \tilde{v}_o \tag{18}$$

Bar sign shows the average component, and tilde sign shows ripple component. And Eq. (25) will result

$$\overline{v}_{ab} + \tilde{v}_{ab} = L\frac{d\overline{i}_L}{dt} + L\frac{d\tilde{i}_L}{dt} + \overline{v}_o + \tilde{v}_o \tag{19}$$

Separating average from ripple component will result,

$$\overline{v}_{ab} = L\frac{d\overline{i}_L}{dt} + \overline{v}_o \tag{20}$$

$$\tilde{v}_{ab} = L\frac{d\tilde{i}_L}{dt} + \tilde{v}_o \tag{21}$$

The capacitor ripple voltage in Eq.(31) is far less than other part, therefore can be simplified to,

$$\tilde{v}_{ab} \approx L\frac{d\tilde{i}_L}{dt} \tag{22}$$

Hence, output ripple current is stated as

$$\tilde{i}_L = \frac{1}{L}\int \left(v_{ab} - \overline{v}_{ab}\right)dt \tag{23}$$

and the rms value of output ripple current can be calculated with the equation,

$$\tilde{I}_{L,rms} = \sqrt{\frac{1}{T}\int_{t_0}^{t_0+T_s} \tilde{i}_L{}^2 .dt} \tag{24}$$

Then, we can obtain

$$\tilde{I}_{L,rms} = \frac{E_d}{L\,f_s}\frac{\alpha(1-\alpha)}{4\sqrt{3}} \tag{25}$$

Where α is converter ratio, $\alpha = D_1 + D_1$, and f_s is switching frequency of dc-dc converter.

The following part will discuss voltage ripple analysis of large ratio dc-dc converter. Current through the capacitor is stated by

$$i_C = i_L - i_O \tag{26}$$

And as explained before, the equation become,

$$\bar{i}_C + \tilde{i}_C = \bar{i}_L + \tilde{i}_L - \bar{i}_O - \tilde{i}_O \tag{27}$$

With

$$\tilde{i}_C = \tilde{i}_L - \tilde{i}_O \tag{28}$$

$$\bar{i}_C = \bar{i}_L - \bar{i}_O \tag{29}$$

The capacitor ripple voltage in Eq.(38) is far less than other part, therefore can be simplified to,

$$\tilde{i}_C \approx \tilde{i}_L \tag{30}$$

Hence, capacitor voltage ripple can be calculated as

$$\tilde{v}_o = \frac{1}{C}\int \tilde{i}_C dt = \frac{1}{C}\int \tilde{i}_L dt \tag{31}$$

and the rms value of capacitor ripple voltage can be calculated with the equation,

$$\tilde{V}_{o,rms} = \sqrt{\frac{1}{T}\int_{t_0}^{t_0+T_s} \tilde{v}_o{}^2 .dt} \tag{32}$$

Then we can obtain,

$$\tilde{V}_{o,rms} = \frac{1}{LC}\frac{E_d}{48\sqrt{5}f_s^2}\alpha(1-\alpha)\sqrt{\left(1+2\alpha-2\alpha^2\right)} \tag{33}$$

Input Ripple Analysis

To analyze the input ripple, some assumptions as stated before also will be taken into account. Fig. 5 shows large ratio dc-dc converter with LC filter in input side for input ripple analysis. Input side waveform details are shown in Fig. 6 (a). i_D is current through S_1 switch, i_{Ls} is inductor current, v_{Cs} is input capacitor voltage.

From Fig. 6 (a), average input current $\bar{i}_d$ is

$$\bar{i}_d = \frac{2}{T_s}\int_{t_0}^{t_{2.5}} i_d \, dt = \alpha I_0 \tag{34}$$

and rms value for input current is,

$$I_d^2 = \frac{2}{T_s}\int_{t_0}^{t_{2.5}} i_d^2 \, dt \tag{35}$$

$$= \alpha I_o^2$$

Then, the value of input current ripple is,

$$\tilde{i}_D = I_o\sqrt{\alpha-\alpha^2} \tag{36}$$

Based on the Eq.(46), it can be seen that input current ripple is independent with switching frequency.

The capacitor current ripple is

$$\tilde{i}_{Cs} = \tilde{i}_{Ls} - \tilde{i}_D \tag{37}$$

Because the current ripple in source inductor is far less then input current ripple, then

$$\tilde{i}_{Cs} = -\tilde{i}_D = -\left(i_D - \bar{i}_D\right) \tag{38}$$

From Eq.(48), then the capacitor voltage ripple can be calculated with

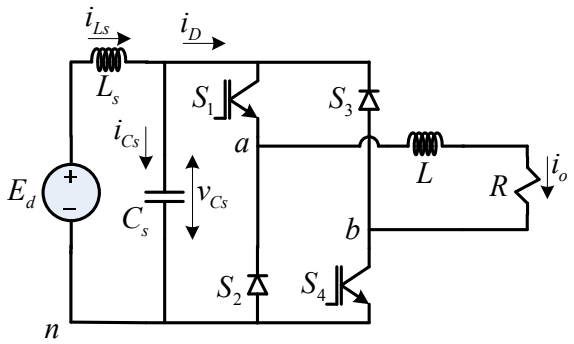


Fig. 5. Large ratio buck dc-dc converter with Ls and Cs.

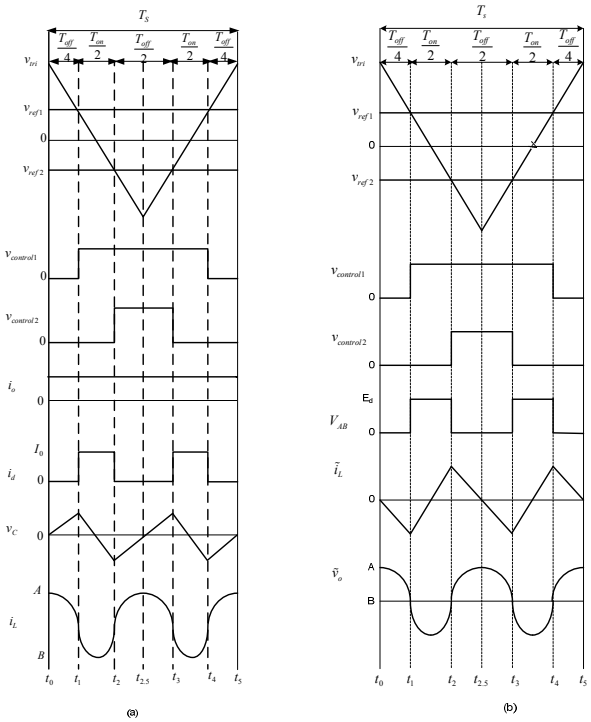


Fig. 6. Ripple waveform details (a) input, and (b) output side.

$$\tilde{v}_{Cs} = \frac{1}{C_s}\int \tilde{i}_{Cs}\, dt \tag{39}$$

And the rms value is

$$\tilde{V}_{Cs} = \frac{2}{T_s}\sqrt{\int_{t_0}^{t_0+\frac{T_s}{2}} \tilde{v}_{Cs}^2 dt} \tag{40}$$

Hence,

$$\tilde{V}_{Cs} = = \frac{I_o}{C_s f_s}\frac{(1-\alpha)\,\alpha}{4\sqrt{3}} \tag{41}$$

To analyze input side inductor current ripple, input side voltage equation can be written as,

$$E_d = L_s \frac{di_{Ls}}{dt} + v_{Cs} \tag{42}$$

If $i_L = \bar{i} + \tilde{i}$, then

$$E_s = L_s \frac{d\bar{i}_L}{dt} + \bar{v}_c \tag{43}$$

$$0 = L_s \frac{d\bar{i}_L}{dt} + \bar{v}_c \tag{44}$$

The source ripple current equation is

$$\tilde{i}_L = -\frac{1}{L_s}\int \tilde{v}_c dt \tag{45}$$

Hence,

$$\tilde{i}_L = \frac{I_o}{2L_s C_s}\begin{cases} (1-\alpha)\,\alpha\left(\frac{T_2}{2}\right)^2\left(\frac{2\alpha+1}{6}\right) \\ \quad -\alpha(t-t_0)^2 & \text{saat } t_o \le t \le t_1 \\ (1-\alpha)\,\alpha\left(\frac{T_2}{2}\right)^2\left(\frac{2\alpha+1}{6}\right) \\ \quad +\left((t-t_1)^2-(t-t_1)\frac{T_{ON}}{2}\right)(1-\alpha) & \text{saat } t_1 \le t \le t_2 \\ (1-\alpha)\,\alpha\left(\frac{T_2}{2}\right)^2\left(\frac{2\alpha+1}{6}\right) \\ \quad -\left(\alpha(t-t_2)^2-(t-t_2)\,\frac{T_{ON}}{2}(1-\alpha)\right) & \text{saat } t_2 \le t \le t_{2.5} \end{cases} \tag{46}$$

Rms value of input inductor current ripple can be calculated with equation,

$$\tilde{I}_{Ls} = \frac{2}{T_s}\sqrt{\int_{t_0}^{t_0+\frac{T}{2_s}} \tilde{i}_{Ls}^2 dt} \tag{47}$$

Hence,

$$\tilde{I}_{Ls} = \frac{I_o(1-\alpha)\,\alpha\sqrt{1+2\alpha-2\alpha^2}}{48\sqrt{5}L_s C_s f_s^2} \tag{48}$$

B. *Losses Analysis*

The losses of DC-DC converter created by switching devices are divided into two losses. First is switching loss, and second is conduction loss.

Switching and conduction losses can be seen in Fig. 7. These waveforms are occurred in inductive circuit with high duty cycle of switching. The circuit is inductive because it contains inductor as current source to make sure current flows to the load every time.

Area 1 is the loss when the current flow is rising, area 2 is the loss when the current flows in the reverse direction through the diode, and area 3 is charge in diode (q_{rr}). These areas are causing high power dissipation in the transistor (switching device).

Switching loss occurs in transistors during the transition from the OFF to ON state (turn-on) and the ON to OFF state (turn-off). The equation of switching losses is given[4]:

$$p_{S\_ON} = \frac{1}{2} E_d I_o t_r f_s + E_d I_o t_{rr} f_s + E_d f_s q_{rr} \tag{49}$$

for turn-on losses, and

$$p_{S\_OFF} = \frac{1}{2} E_d f_s I_o t_{cf} \tag{50}$$

for turn-off losses, where

Ed = Supply voltage
Fs = Switching frequency
Io = Output current
t_r = Switching device current rise time
t_{rr} = Diode reverse recovery time
q_{rr} = Diode reverse recovery charge
t_{cf} = Switching device turn-off recovery time

In most intended operating currents, it is more appropriate to assume that the transistor current rise time and turn-off crossover time and the diode reverse recovery time and charge are made up of a constant component plus a component that is linierly dependent upon current[4], that is

$$t_r = T_r + C_{tr} I_o \tag{51}$$
$$t_{cf} = T_{cf} + C_{cf} I_o \tag{52}$$
$$t_{rr} = T_{rr} + C_{rr} I_o \tag{53}$$
$$q_{rr} = Q_{rr} + C_{qr} I_o \tag{54}$$

The switching loss, therefore, can be written as

$$p_S = p_{S\_ON} + p_{S\_OFF} \tag{55}$$
$$p_S = \frac{1}{2} E_d f_s \left(C_0 + C_1 I_o + C2 I_o^2 \right) \tag{56}$$

where

$$C_0 = 2Q_{rr} \tag{57}$$
$$C_1 = T_r + T_{cf} + 2T_{rr} + 2C_{qr} \tag{58}$$
$$C_2 = C_{tr} + C_{cf} + 2C_{rr} \tag{59}$$

Conduction loss occures due to voltage drops across transistors and diodes during conduction. These voltages which are functions of the current that flows through them cn be approximated as the following linear functions:

$$v_T = V_T + R_T I_S \tag{60}$$

for transistors, and

$$v_D = V_D + R_D I_S \tag{61}$$

for diodes.

Conduction losses are the product of the ON state voltage of the switching device and the current flowing through it.

The equation of conduction losses is then

$$p_T = V_T \bar{I}_S + R_T I_{S\,rms}^2 \tag{62}$$

for transistor, and

$$p_D = V_D \bar{I}_S + R_D I_{S\,rms}^2 \tag{63}$$

for diode, where

R_T / R_D = Switching device's resistance.
V_T / V_D = ON state voltage.
Is = Current flow through switching device

To achieve the losses equation, then we must calculate the average and rms value of current flowing through each switches.

Average values are,

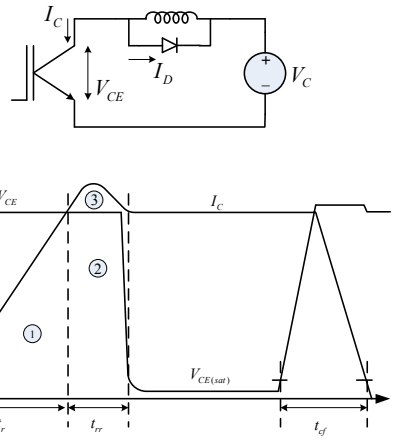


Fig. 7. Model of switching waveforms during turn-on and turn-off.

$$\bar{I}_{S1} = \frac{T_{onS1}}{T_{sS1}} I_o = D_1 I_o \tag{64}$$

$$\bar{I}_{S2} = \frac{T_{offS1}}{T_{sS1}} I_o = (1 - D_1) I_o \tag{65}$$

$$\overline{I}_{S3} = \frac{T_{onS3}}{T_{sS3}} I_o = D_2 I_o \tag{66}$$

$$\overline{I}_{S4} = \frac{T_{offS3}}{T_{sS3}} I_o = \left(1 - D_2\right) I_o \tag{67}$$

Where T_{onS1} and T_{onS3} are ON time for S_1 and S_3; T_{offS1} are T_{offS3} are OFF time S_1 and S_3; T_{sS1} and T_{sS3} are switching period for S_1 and S_3; D_1 and D_2 are *duty cycle* for each S_1 and S_3.

The rms values are

$$I_{S1,rms} = \sqrt{\frac{1}{T_{sS1}} \int_0^{T_{onS1}} I_o^2 dt} = \sqrt{D_1} I_o \tag{68}$$

$$I_{S2,rms} = \sqrt{\left(1 - D_1\right)} I_o \tag{69}$$

$$I_{S3,rms} = \sqrt{D_2} I_o \tag{70}$$

$$I_{S4,rms} = \sqrt{\left(1 - D_2\right)} I_o \tag{71}$$

From Eq.(74)-(81), we can obtain total switching loss,

$$P_s = \frac{1}{2} E_d f_s \left(2C_0 + C_1 \left(1 + \alpha\right) I_o + C_2 \left(1 + \alpha\right) I_o^2\right) \tag{72}$$

and total conduction loss,

$$P_c = V_T \left(1 + \alpha\right) I_o + R_T \left(1 + \alpha\right) I_o^2 + V_D \left(1 - \alpha\right) I_o + R_D \left(1 - \alpha\right) I_o^2 \tag{73}$$

Hence, the total losses is

$$P_S = P_s + P_c \tag{74}$$

$$P_S = \begin{pmatrix} \frac{1}{2} E_d f_s \left(2C_0 + C_1 \left(1 + \alpha\right) I_o + C_2 \left(1 + \alpha\right) I_o^2\right) + \\ V_T \left(1 + \alpha\right) I_o + R_T \left(1 + \alpha\right) I_o^2 + V_D \left(1 - \alpha\right) I_o + R_D \left(1 - \alpha\right) I_o^2 \end{pmatrix} \tag{75}$$

C. Comparison

The equations for those performances in two-phase and three-level dc-dc converter are shown in Table 1 and Table 2. To simplify the comparison, the results obtained in Table 1 and 2, are drawn. Fig. 8 shows source current ripple, and Fig.9 shows it in extreme duty cycle. Fig. 10 shows output current ripple, and Fig. 11 shows it in extreme duty cycle.

Fig.12 shows the total loss comparison between three dc-dc converters. It can be seen that large ratio dc-dc converter results the largest loss for all duty cycle. In large ratio dc-dc converter, current flows through two switches. Therefore, large ratio dc-dc converter has bad performance in loss aspect.

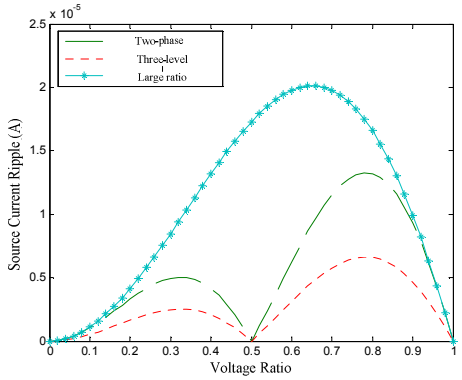


Fig. 8. Source current ripple comparison.

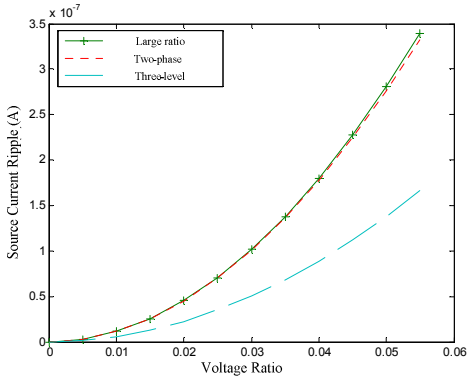


Fig. 9. Source current ripple comparison for extreme voltage ratio.

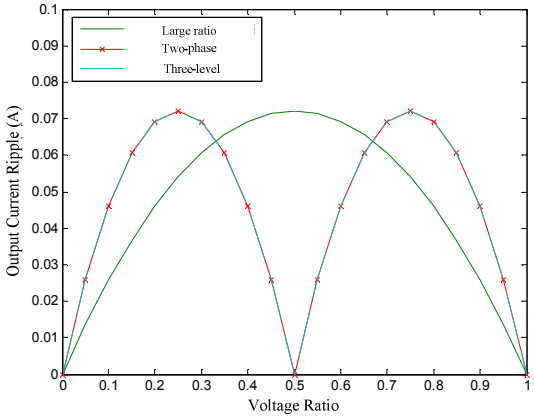


Fig. 10. Output current ripple comparison.

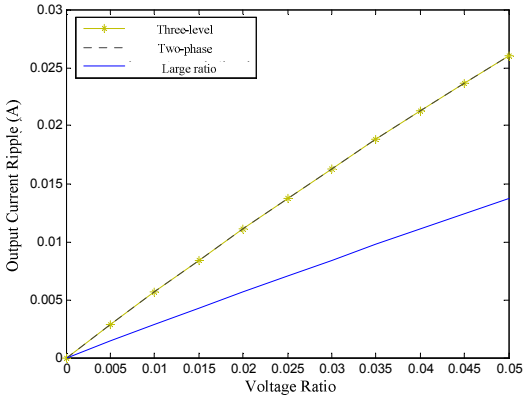


Fig. 11. Output current ripple for extreme voltage ratio.

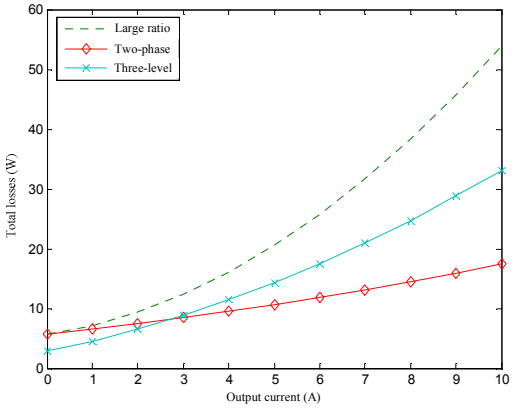


Fig. 12. Total losses comparison.

4. Control Technique for Large Ratio Dc-Dc Converter

Current controller has been used in many converter applications[6]-[8]. Current control has the advantage in current protection especially when short circuit occurred. In addition, the use of current controller enables parallel operation of two or more similar converters. Thus the power capacity can be increased. Commonly, in dc-dc converter applications, the current control is used in double-loop controller. In this scheme, voltage controller is in the outer loop while current controller is in the inner loop. The output of voltage controller will be the input for current controller.

In the proposed controller, hysteresis current controller is used while PI controller is used as voltage controller as can be seen in Fig. 13. The error signal between output and reference voltage will be the input for hysteresis current controller. The output signal from hysteresis current controller will determine switching signals. Since two separated switching signals are required, additional logic circuit is needed to produce these signals from hysteresis output signal.

Whenever output voltage is lower than reference voltage, the required inductor current will be increased. Hence, the duty cycle will be increased. In contrast, the duty cycle will be decreased whenever output voltage is higher than reference voltage in which the inductor current will be lessened. In order to maintain well operation, the current controller has to be faster in response than the voltage controller. The proposed control technique block diagram is

shown in Fig. 14.

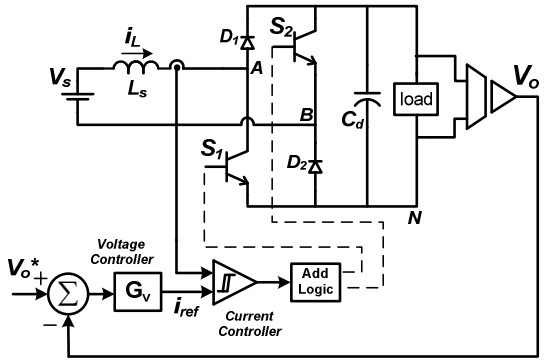


Fig. 13 Control technique for high ratio boost converter.

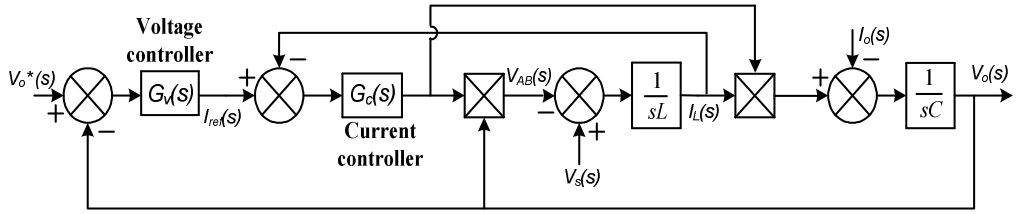


Fig. 14 Block diagram of control system in high ratio boost converter.

The simplicity and stability of hysteresis controller is applied in the proposed control technique. Basically, hysteresis current controller is the controller in which the allowed error signal is limited to the given hysteresis band. If the inductor current exceeds the upper band limit, then the switch is off and the current is decreasing. Then if the inductor current exceeds the lower band limit, the switch turn on provided the rising in current. The process keeps on going so as to keep the inductor current follows the hysteresis band path (Fig. 15).

The instantaneous inductor current can be written as the sum of average component and ripple component as follow:

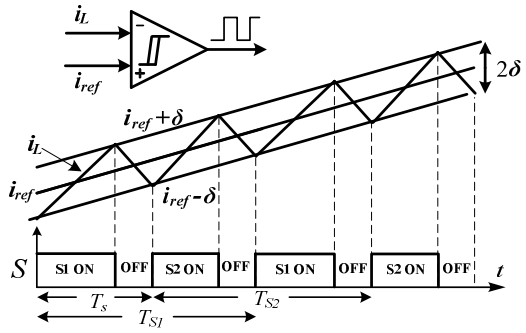


Fig. 15 Current controller with hysteresis band in boost converter.

$$i_L = \overline{i_L} + i_L \tag{76}$$

where $\overline{i_L}$ *and* i_L are average and ripple component of inductor current respectively. Fig. 15 depicts that the average inductor current is equal to the reference while the maximum inductor current ripple is ±δ, where δ is hysteresis half band and can be expressed as:

$$\overline{i_L} \pm i_{L\max} \; i_{ref} \pm \delta \tag{77}$$

In boost converter the inductor current can be written as follow:

$$i_L = \frac{1}{L}\int \left(v_S - v_O\right) dt + i_{L0} \tag{78}$$

where i_{L0} is the initial inductor current. When the switch is on then v_o in (78) is zero, hence the inductor current is as follow:

$$i_L = \frac{v_S}{L} t + \left(\overline{i_L} - \delta\right) \text{ ; for } 0 < t < T_{ON} \tag{79}$$

From Eq. (77) and (79), we get T_{ON} switch as follow

$$T_{ON} = \frac{2\delta L}{v_S} \tag{80}$$

Inductor current when the switch is off can be written as

$$i_L = \frac{v_S - v_O}{L} t + \left(\overline{i_L} + \delta\right) \text{ ; for } 0 < t < T_{OFF} \tag{81}$$

Note that in (81) the output voltage is bigger than input voltage; therefore the inductor current will decrease. From equations (77) and (81), we get T_{OFF} of the switch as

$$T_{OFF} = \frac{2\delta L}{v_O - v_S} \tag{82}$$

As boost converter, then the requirement is

$$k_1 + k_2 < 1 \tag{83}$$

To minimize current ripple caused by switching process, then

$$k_1 = k_2 \tag{84}$$

For balancing the switching patterns and fulfilling the Eq. (83) – (84), so

$$T_{S1} = T_{S2} = 2T_S = 2\left(T_{ON} + T_{OFF}\right) = \frac{4v_O \delta L}{v_S\left(v_O - v_S\right)} \tag{85}$$

From Eq (85), the operation frequency can be written as

$$f_{S1} = f_{S2} = \frac{1}{4\delta L}\left(\frac{\alpha - 1}{\alpha}\right) \text{ ; with } \alpha = v_o / v_s \tag{86}$$

For extreme input-output ratio, the switching frequency can be approximated to

$$f_S \approx \frac{1}{4\delta L} \tag{87}$$

The switching signals in both switches are differed and separated. In order to keep the balance and one after another operation of switching signals, logic circuit is required to be added to hysteresis current controller. Thus, it can be obtained that

$$T_{ON1} = T_{ON2} \tag{88}$$

$$\begin{aligned} t_1 &= t_1 + n\left(2T_S\right) \; ; n = 0, 1, 2, ... \\ t_2 &= t_2 + n\left(2T_S\right) \; ; n = 0, 1, 2, ... \end{aligned} \tag{89}$$

$$\begin{aligned} t_1 &= t_2 + \left(2n+1\right)T_S \; ; n = 0, 1, 2, ... \\ t_2 &= t_1 + \left(2n+1\right)T_S \; ; n = 0, 1, 2, ... \end{aligned} \tag{90}$$

Where T_{Sx} and t_x are switching period and state at the time t respectively. From equations (89) and (90) it can be seen that the switching signals are never collided.

Because of the hysteresis control system used is non-linear; the simplification can be done to ease the analysis. In designing the voltage controller we can assume that the current controller is well-operated provided the reference is equal to the inductor current. The output voltage of boost converter can be expressed as follow:

$$\begin{aligned} v_O &= -\frac{1}{C}\int i_O dt \; ; \text{untuk } 0 < t < T_{ON} \\ v_O &= \frac{1}{C}\int \left(i_L - i_O\right) dt \; ; \text{untuk } 0 < t < T_{OFF} \end{aligned} \tag{91}$$

With the assumed well-operated current controller, the block diagram in

Fig. 14 can be simplified to the one in Figure 16. From the figure, $G_c^*(s)$ is '1' when the switch is on and '0' when the switch is off. The consequence of this condition made the proposed voltage controller is non-linear. To simplify the analysis, the linearization process can be used.

Eq. (91) can be written as

$$C\frac{dv_O}{dt} = \left(1-k\right)i_L - i_O \tag{92}$$

where k is the various duty factor and can be express as

$$k = \bar{k} + \tilde{k} \tag{93}$$

with the sign '~' indicate the ripple component with the properties as follow:

$$\begin{aligned} \tilde{k} &= \left(1-\bar{k}\right) \; ; \; 0 < t < T_{ON} \\ \tilde{k} &= -\bar{k} \; ; \; T_{ON} < t < T_S \end{aligned} \tag{94}$$

We can express the Eq. (92) in respect to the voltage ratio for boost converter as

$$C\frac{dv_O}{dt} = \left(\alpha^*\right)i_L - i_O \; ; \; \alpha^* = \frac{v_S}{v_O} \tag{95}$$

Splitting the Eq. (95) to the average and ripple component we can get

$$C\frac{d(\bar{v}_o + v_o)}{dt} = (\overline{\alpha^*} + \alpha^*)(\bar{i}_L + i_L) - (\bar{i}_o + i_o) \tag{96}$$

Because of average component in the left side of the equation is zero, and assuming that the multiplication of ripple components is negligible, we can express Eq. (96) as

$$C\frac{dv_o}{dt} = (\overline{\alpha^*}.i_L) + (\alpha^*.\overline{i_L}) - (i_o) \tag{97}$$

The Eq. (97) is valid for small signal analysis. Using the above equation, the response of output voltage because of small duty cycle or load deviation can be analyzed. For each response, we get

$$\frac{v_o(s)}{\alpha^*(s)} = \frac{\overline{I_L}}{sC + \overline{\alpha^*}.G_v(s)} \tag{98}$$

$$\frac{v_o(s)}{I_o(s)} = -\frac{1}{sC + \overline{\alpha^*}.G_v(s)} \tag{99}$$

From Eq. (97), the block diagram can be redrawn as can be seen in Figure 16.

The proposed voltage controller is the commonly used *proportional-integral* (PI). This PI controller can eliminate steady-state error. We can get the desired transient and steady-state response using the optimally adjusted control system parameter. Applying proportional and integral constant to $G_v^*(s)$ in Figure 16 we can get output voltage response in respect to reference and load current as follow:

$$\frac{V_o(s)}{\alpha^*(s)} = -\frac{s\overline{I_L}}{s^2C + s\overline{\alpha^*}K_p + \overline{\alpha^*}K_i} \tag{100}$$

$$\frac{V_o(s)}{I_o(s)} = -\frac{s}{s^2C + s\overline{\alpha^*}K_p + \overline{\alpha^*}K_i} \tag{101}$$

Using switching frequency of 2kHz and hysteresis band of 400mA, from (87) we get the inductance L_s as large as 0.625mH. In order to make the voltage controller response slower than the current controller, we can take the minimum criteria in which current controller response is ten times greater than voltage controller response. Hence, using system parameter C = 220μF, it is obtained that K_p = 0.2 and K_i = 2000 in which the good transient response can be obtained. Bode diagram of output voltage response in respect to the duty cycle and load current changes can be seen in Fig. 17.

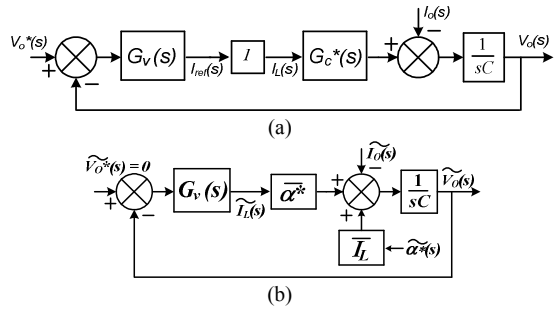
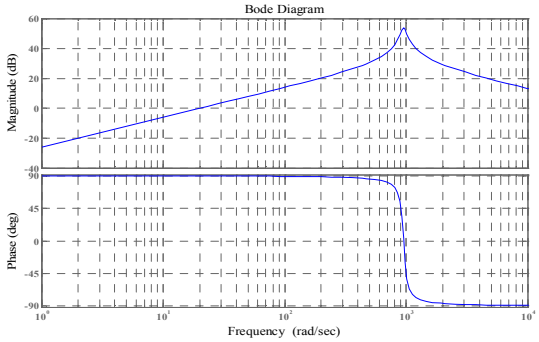
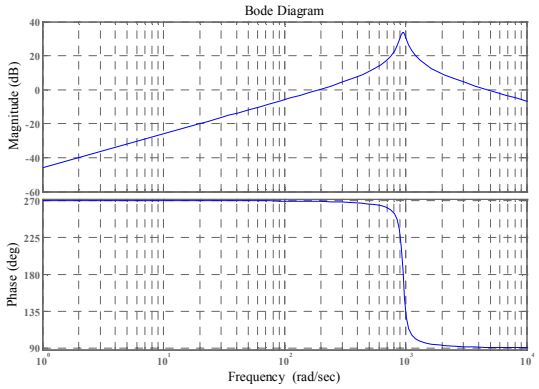


Figure 16 (a) voltage controller block diagram and (b) simplified voltage controller block diagram



(a)



(b)

Fig. 17 (a) bode diagram of output voltage response vs. duty cycle and (b) load current

5. Experimental Results

In order to verify the proposed topology, a small proposed large ratio dc-dc converter topology has been constructed based on Fig. 2(e) for buck converter and Fig. 3 for boost converter.

A. Ripple Analysis

Fig. 18 and Fig. 19 show experimented result of output current ripple and source current ripple in large ratio buck dc-dc converter. As can be seen, the experimented results appropriate to the calculated results.

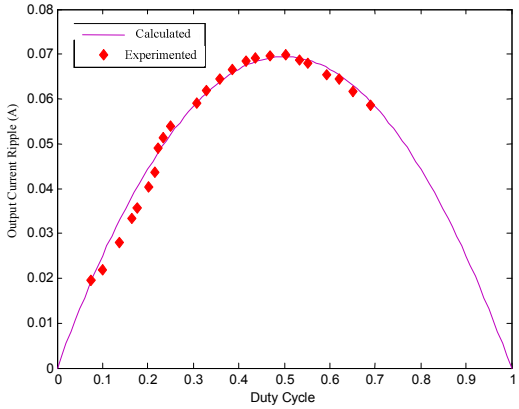


Fig. 18. Experimented result of output current ripple.

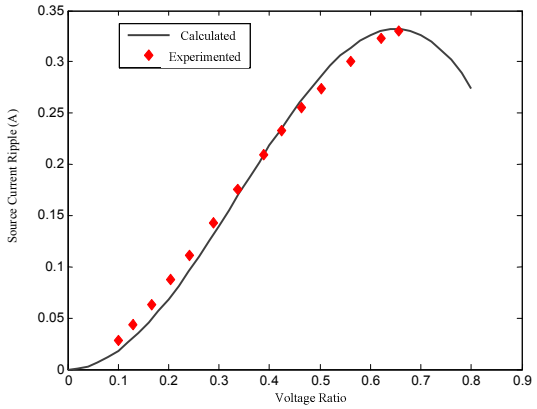


Fig. 19. Experimented result of source current ripple.

B. Loss Analysis

Fig. 20 shows the experimented result compared with calculated result. As can be seen that the experimented result approaching the calculated result. The differences are caused by either inaccurate parameter and output current contains ripple in experiment.

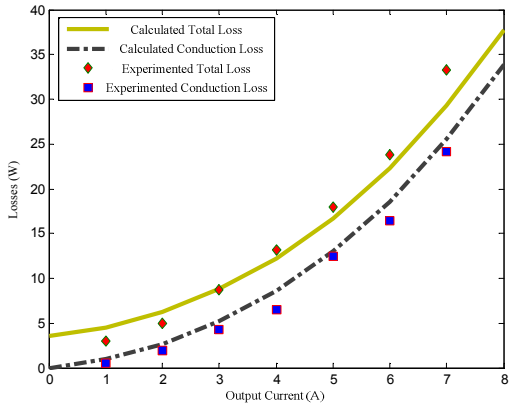


Fig 20. Experimented result of total losses.

C. Control Technique

Experiments is done to see the system response as the consequence of load disturbance and reference voltage changes. In current controller, current sensor used has the parameter of 2A/V and hysteresis band of 400mA. Experiment results for load disturbances can be seen in Fig. 21. With the existence of load disturbance, the output voltage is constant.

The experiment results using input voltage with some ripple component is drawn in Fig. 22. We can see that output voltage is not altered by high frequency ripple components in input voltage. With the reference voltage changed, experiment results is as can be seen in Fig. 23. In the low frequency, the output voltage will follow the voltage given by the reference. But in higher frequency, the output voltage cannot follow the reference anymore.

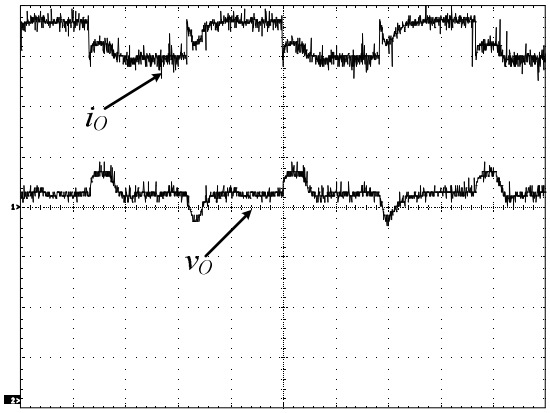


Fig. 21 Output voltage signal (25V/div) when load is changed (500mA/div) at 250ms/div.

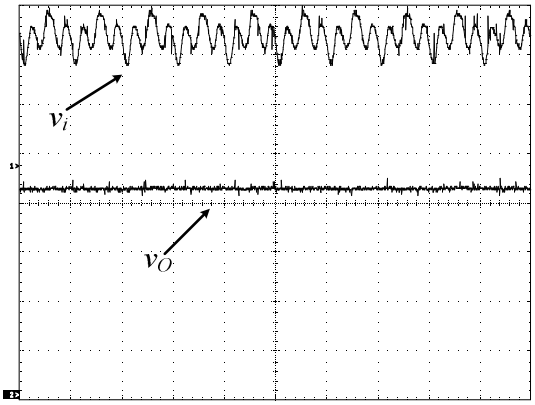


Fig. 22 Output voltage signal (25V/div) when input voltage contain some ripple (5V/div) at 10ms/div.

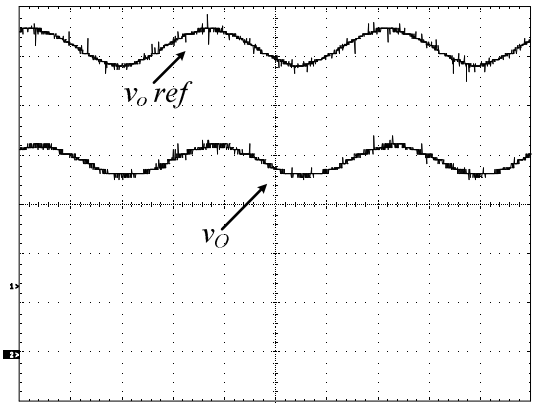


Fig. 23 Output voltage signal (25V/div) in respect to reference (20V/div) at 250ms/div.

6. Conclusions

A large ratio dc-dc converter topology is derived. This high ratio dc-dc converter topology is able to convert its input voltage into very small/big output voltage without need to operate its switching devices in the extreme duty cycle as in the conventional dc-dc converter.

Analytic equation for input and output ripple of large ratio has been discussed. At extreme voltage ratio, large ratio dc-dc converter has smaller or equal ripple than two-phase and three-level dc-dc converter. Analytic equation of switching and conduction losses has been derived. The total loss of large ratio dc-dc converter is larger than the others.

Control technique of large ratio boost dc-dc converter has been discussed. Double loop control technique with hysteresis current controller and PI voltage controller is proven to work well in existence of load disturbance to maintain output voltage.

Large ratio boost dc-dc converter is appropriate for renewable energy power generator with low dc voltage output. Experimental result has been included to verify the proposed topology.

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Parameter	Two-Phase	Three-level	Large ratio
Output Current Ripple ($\tilde{I}_o$)	for $0 \le \alpha \le 1/2$ $\frac{E_d}{(L_2)\, f_s}\frac{\alpha(1-2\alpha)}{2\sqrt{3}}$ for $1/2 \le \alpha \le 1$ $\frac{E_d}{(L_2) f_s}\frac{(1-\alpha)(2\alpha-1)}{2\sqrt{3}}$	for $0 \le \alpha \le 1/2$ $\frac{E_d}{L\, f_s}\frac{\alpha(\alpha^2-\alpha+0.25)^{\frac{1}{2}}}{4\sqrt{3}}$ for $1/2 \le \alpha \le 1$ $\frac{E_d}{L\, f_s}\frac{(1-\alpha)(2\alpha-1)}{4\sqrt{3}}$	$\frac{E_d}{L\, f_s}\frac{\alpha(1-\alpha)}{4\sqrt{3}}$
Output Voltage Ripple	if $0 \le \alpha \le 1/2$: $\frac{E_d}{f_s^2 C(L+M)}\frac{\alpha(1-2\alpha)(1+4\alpha-8\alpha^2)^{1/2}}{24\sqrt{5}}$ if $1/2 \le \alpha \le 1$: $\frac{E_d}{f_s^2 C(L+M)}\frac{(1-\alpha)(2\alpha-1)(-3+12\alpha-8\alpha^2)^{1/2}}{24\sqrt{5}}$		$\frac{1}{LC}\frac{E_d}{48\sqrt{5}f_s^2}\alpha(1-\alpha)\sqrt{\left(1+2\alpha-2\alpha^2\right)}$
Source Current Ripple ($\widetilde{I}_L$)	for $0 \le \alpha \le 1/2$ $\left[\frac{I_o(1-2\alpha)\alpha}{L_s C_s f_s^2}\right]\frac{\sqrt{1+4\alpha-8\alpha^2}}{48\sqrt{5}}$ for $1/2 \le \alpha \le 1$ $\left[\frac{I_o(2\alpha-1)(1-\alpha)}{L_s C_s f_s^2}\right]\frac{\sqrt{-3+12\alpha-8\alpha^2}}{48\sqrt{5}}$	for $0 \le \alpha \le 1/2$ $\left[\frac{2I_o(1-2\alpha)\alpha}{L_s C_s f_s^2}\right]\frac{\sqrt{1+4\alpha-8\alpha^2}}{48\sqrt{5}}$ for $1/2 \le \alpha \le 1$ $\left[\frac{2I_o(2\alpha-1)(1-\alpha)}{L_s C_s f_s^2}\right]\frac{\sqrt{-3+12\alpha-8\alpha^2}}{48\sqrt{5}}$	$\left[\frac{I_o(1-\alpha)\alpha}{8L_s C_s f_s^2}\right]\sqrt{\frac{1+2\alpha-2\alpha^2}{180}}$

Table 1. Ripple equations for dc-dc converters.

rameter	Two-Phase	Three-level	Large ratio
itching ses	$E_d f_s\left(C_0+\frac{1}{2}C_1 DI_o+\frac{1}{4}C_2 DI_o^2\right)$	$\frac{1}{2}E_d f_s\left(C_0+C_1 DI_o+C_2 DI_o^2\right)$	$\frac{1}{2}E_d f_s\left(2C_0+C_1\left(1+D\right)I_o+C_2\left(1+D\right)I_o^2\right)$
nduction ses	$\left(V_T DI_o+\frac{1}{2}R_T DI_o^2+V_D\left(1-D\right)I_o+\frac{1}{2}R_D\left(1-D\right)I_o^2\right)$	$\left(2V_T DI_o+2R_T DI_o^2+2V_D\left(1-D\right)I_o+2R_D\left(1-D\right)I_o^2\right)$	$\left(V_T\left(1+D\right)I_o+R_T\left(1+D\right)I_o^2+V_D\left(1-D\right)I_o+R_D\left(1-D\right)I_o^2\right)$
al ses	$\left(E_d f_s\left(C_0+\frac{1}{2}C_1 DI_o+\frac{1}{4}C_2 DI_o^2\right)+V_T DI_o+\frac{1}{2}R_T DI_o^2+V_D\left(1-D\right)I_o+\frac{1}{2}R_D\left(1-D\right)I_o^2\right)$	$\left(\frac{1}{2}E_d f_s\left(C_0+C_1 DI_o+C_2 DI_o^2\right)+2V_T DI_o+2R_T DI_o^2+2V_D\left(1-D\right)I_o+2R_D\left(1-D\right)I_o^2\right)$	$\left(\frac{1}{2}E_d f_s\left(2C_0+C_1\left(1+\alpha\right)I_o+C_2\left(1+\alpha\right)I_o^2\right)+V_T\left(1+\alpha\right)I_o+R_T\left(1+\alpha\right)I_o^2+V_D\left(1-\alpha\right)I_o+R_D\left(1-\alpha\right)I_o^2\right)$

Table 2. Losses equations for dc-dc converters.