

Comparison Study and Simulation of the Main Multilevel Inverter Topologies for Different Output Voltage Levels

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Abstract: This paper discusses the difference between the three fundamental types of multilevel inverter (MLI) topologies, which are the neutral-point-clamped, the flying capacitors and the cascaded H-bridges. The sinusoidal pulse width modulation technique was used to simulate the output voltages and currents of the MLI inverters. The total harmonic distortion (THD) was estimated for each topology and each voltage level. Moreover, the simulation results indicate that the cascaded structure exhibited a lower THD value even when increasing the number of the output voltage. Furthermore, a new key parameter was defined as cost efficiency factor and used to compare the three topologies. Evaluation results of this factor indicate that the cascaded structure was the most advantages as it reduces stress effect on the inverter switches by eliminating the power diodes and capacitors.

Keywords: Multilevel Inverter, Sinusoidal Pulse-width modulation, Cost efficiency

1. Introduction

The fast growth of PV power application industry requires the development of new technologies to maximize the energy yield of the PV systems [1]. This technology concerns the electrical power operation control and transfer in between the PV sources and the customers, to keep the supply of the electric power in a way to match the international standard requirement for power supply [2]. One of the weak points of the PV systems is the incapability conversion from the DC voltage to the AC voltage before connecting to the power network [3]. This conversion is performed by inverters, which are used in power system application and uninterrupted power supplies industries [4]. Improvement of the output voltage required an appropriate control of the waveform on the inverter to reduce its respective harmonic and electromagnetic effect by the diminution of switching operations and hence the filter size [5]. The limitations of the conventional inverters in the case of power or harmonic effect lead to the usage of the multilevel inverter (MLI) technology which promises some advantages over the conventional inverter especially for high power applications [6]. Three main topologies for multilevel inverter are used. The first structure is known as the neutral-point-clamped (NPC) [7], the second as the flying capacitor (FC) [8] and the third as the cascaded H-bridge with separate DC sources [9]. They are characterized by many features such as low total harmonic distortion (THD) of generated output voltage, reduced size of the filter and increased the system efficiency [10]. Thus, aspect lead the MLI topologies to find their application in PV system on the low cost and high performance [11]. New combined topology have been reported, such as three-phase MMLI, where the authors developed to reduce the components number and improve the output voltage level [12]. Moreover, the MLDC topology which is based on cascaded H-bridge topology connected with half H-bridges cells in a series configuration in purpose to reduce the components number. However, this topology shows a high harmonic stress effect on the switches [13]. Various switching strategies of multilevel inverters are categorized into high switching frequency methods such as sinusoidal pulse width modulation (SPWM) strategy [14] and low switching frequency techniques, often equal to the fundamental switching frequency of the

components, which create stepwise output voltage waveform [15]. The second category comprises of three major switching strategies so-called optimized harmonic stepped waveform (OHSW) [16], selective harmonic mitigation (SHM-PWM) [17-18], and optimal minimization of the THD [19]. Selective harmonic elimination is an as efficient method to mitigate the low-order harmonic components [20]. The different form of multilevel cascade inverter reported previously shown a sign of improvement comparable to the two other topologies in term of component reduce [21]-[25], and harmonic distortion decrease [26]-[31].

Despite all the different topologies and switching techniques discussions, there is a lack of data comparing in same research work the three main topologies in term of component number and, or output voltage level and, or total harmonic distortion and their impact on the cost efficiency.

In this paper, a direct comparison between the three different topologies of the multilevel inverter in term of level number and the output voltage is discussed. Including evaluating the dependency of the cost efficiency factor to the inverter type or level, and prove that the MLI cascade topology remains the best choice based on the cost efficiency factor.

2. System Description

In this work, the three traditional topologies of the multilevel inverter with different output voltage level are reviewed. Each topology required several number of separated sources and components depending on the desired levels of voltage. For the control method, SPWM was chosen based on its simplicity and efficiency to deal with more than 3 level output voltage.

A. Case-study MLI circuit

In this paper, four different level of each traditional multilevel inverter we discussed, taking the seven level for each topology as an example circuit for output voltage discussion. Starting with the circuit schematic for the traditional seven level MLI Neutral-point-clamped configuration also known as neutral-diode-clamped as shown in Figure 1.

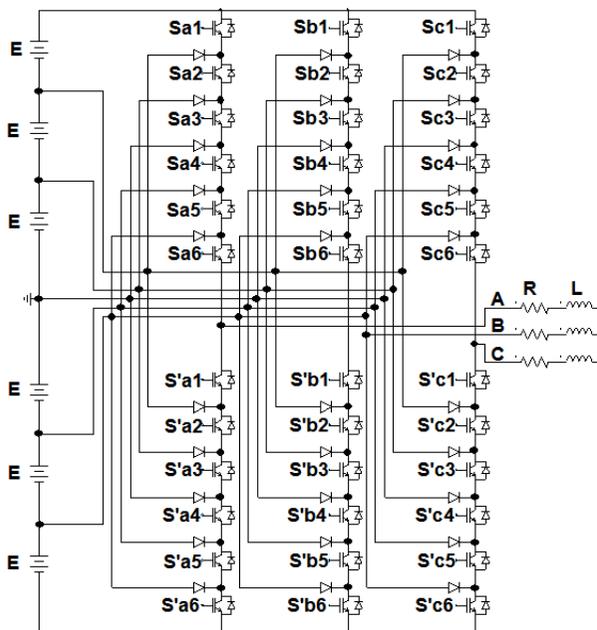


Figure 1. Three phases seven-level NPC topology inverter

The seven-level NPC topology consists of six isolated power sources supply all the circuit with twelve switches in each leg. The switches are operated in complementary (Sa1, S'a1) to

(Sa6, Sa6') mode with high frequency. The number of components for each topology is shown in Table I.

Table 1. Components number of the three studied topology
(Number of switches, Number of Diodes, Number of Capacitors)

	Topology		
	NPC	FC	Cascade
Power Source	$m-1$	1	$3/2(m-1)$
Principal dispositifs of commutation	$6(m-1)$	$6(m-1)$	$6(m-1)$
Diodes	$6(2m-3)$	$6(m-1)$	$6(m-1)$
Capacitors	0	$3m-4$	0
Total number of components	$19m-25$	$15(m-1)$	$13.5(m-1)$

Figure 2 illustrate the circuit schematic of the seven level flying capacitor structure in which capacitors replaced the power diodes of the NPC structure and powered up using only one power source.

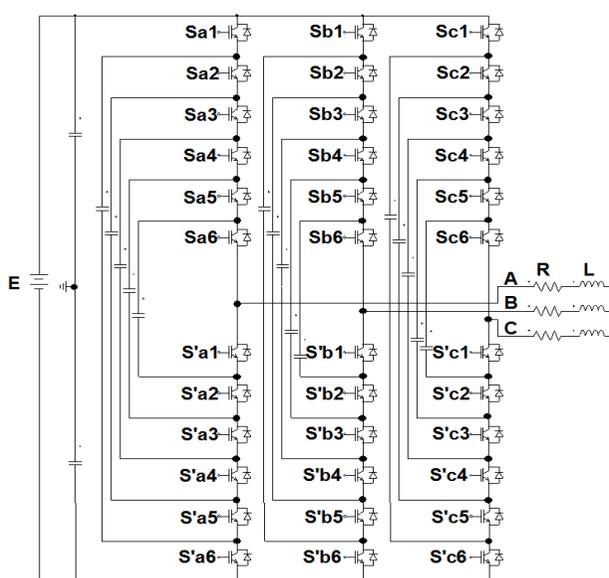


Figure 2. Three phases seven-level FC topology inverter

The third topology with seven level, known as Cascaded MLI is shown in Figure 3; it consists of H-bridge cells powered by separate power supplies and contain in each cell four switches cooperated in parallel mode (Sa1, S'a1), and a total of three cells in each leg. The control detail and output voltages are discussed in the next subsection.

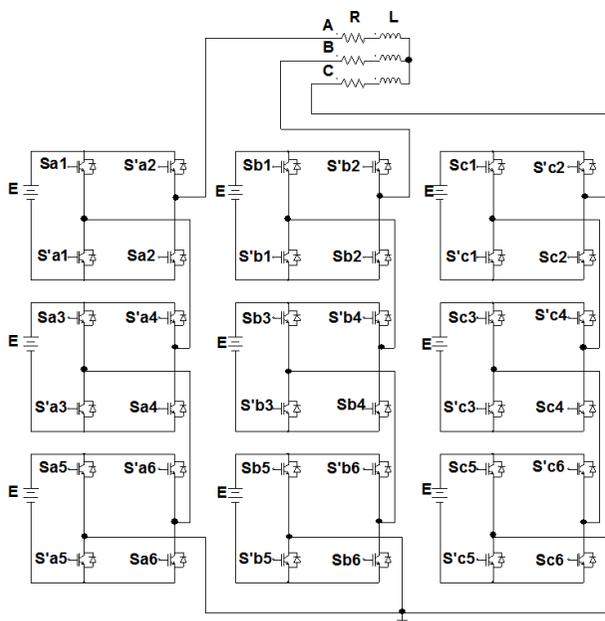


Figure 3. Three phases seven-level Cascaded topology inverter

B. Sinusoidal pulse width modulation (SPWM)

The SPWM is categorized as carrier based modulation strategies; it consists of comparing a sinusoidal signal with high-frequency carrier waveform. The result of comparison generates the control of switches by Boolean signals. Previously, as mentioned, the SPWM achieves the lowest THD on the line-to-line voltage, and it is due to the logical control,³² which is based on the PD control leading all the carrier to be in phase as shown in Figure 4.

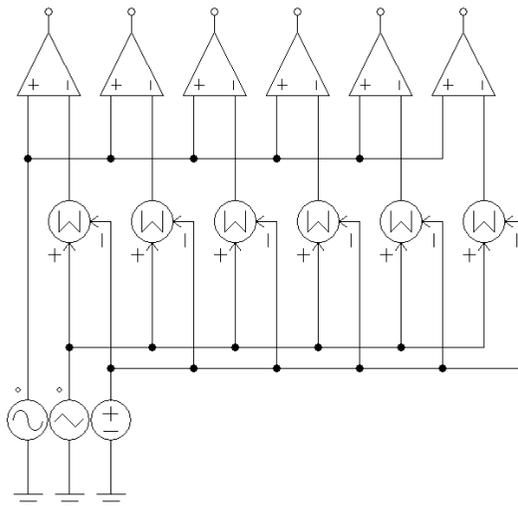


Figure 4. Logical diagram of the SPWM used for the simulation

The output voltage level (n) is given by a comparison of the (n-1) high-frequency carrier signals with a sinusoidal waveform. In this case, the main control signals G1 to G6 are generated by comparing 6 triangular carrier signals with a sinusoidal modulation signal as shown in Figure 5.

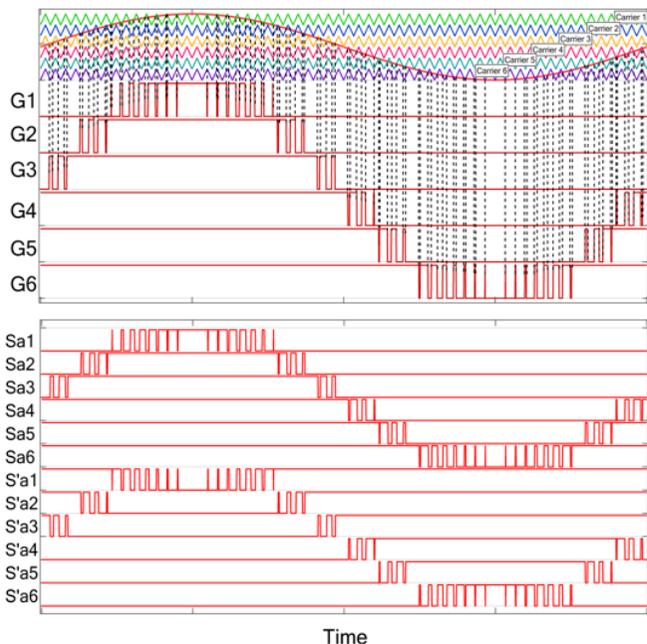


Figure 5. Switching patterns of the used MLI for seven-level

The corresponding monitoring of the switches is done by executing few logical processes. The control results are illustrated in Table II and show the different switching stages of the seven-level MLI controlled by SPWM. The frequency modulation index, which describe the frequency relation between the sinusoidal signal and the carrier signals is given by [6] and its value chosen to be 60 based on previous work.

$$m_f = \frac{f_c}{f_m} \tag{1}$$

Table 2. Different Switching Stages of the used MLI for Seven-level MLI (1=ON, 0=OFF)

V_{AO}	3E	2E	E	0	-E	-2E	-3E
S_{a1}	1	0	0	0	0	0	0
S_{a2}	1	1	0	0	0	0	0
S_{a3}	1	1	1	0	0	0	0
S_{a4}	1	1	1	1	0	0	0
S_{a5}	1	1	1	1	1	0	0
S_{a6}	1	1	1	1	1	1	0
S'_{a1}	0	1	1	1	1	1	1
S'_{a2}	0	0	1	1	1	1	1
S'_{a3}	0	0	0	1	1	1	1
S'_{a4}	0	0	0	0	1	1	1
S'_{a5}	0	0	0	0	0	1	1
S'_{a6}	0	0	0	0	0	0	1

Moreover, the amplitude modulation index also known as the modulation factor which describes the relationship between the carriers amplitude with the sinusoidal amplitude is given by [2]

$$m_i = \frac{A_m}{(m-1)A_c} \tag{2}$$

And, its value chosen to be equal to 1 based on previous work results, ² as shown in Table 3.

Table 3. Specification Simulation Parameters

System Parameters	Value
DC-voltage source $\Sigma(E)$	220 volts
Load value (at 50Hz)	R=20 Ω , X _L =62.8 Ω , X _C =62.8 Ω
Switching Frequency (f _s)	3 KHz
Modulation Index (m _i)	1
Frequency Modulation Index (m _f)	60

3. Simulation and results discussion

Figure 6 shows out line-to-line voltages V_{AB} , V_{BC} , and V_{CA} , which are deduced from the pole voltage by

$$\begin{aligned} V_{AB} &= V_{A0} - V_{B0} \\ V_{BC} &= V_{B0} - V_{C0} \\ V_{CA} &= V_{C0} - V_{A0} \end{aligned} \tag{3}$$

Seven-level in the line-to-line voltage V_{AB} , V_{BC} , V_{CA} , where each one of them is shifted by a phase angle equal to 120° (3E, 2E, E, 0, -E, -2E, -3E), is produced from five-level pole voltages. Nine-level pole voltages produced eleven-level line to line voltages (5E, 4E, 3E, 2E, E, 0, -E, -2E, -3E, -4E, -5E). The pole voltage number [m-2] (m is the number of MLI levels) is used to get [m] line-to-line output voltages, and it was similar in the case of the different topology (NPC, FC, and Cascaded). Furthermore, the ability to feed different load (R-L, R-C) and overall efficiency have been investigating for the different topology with various level, the value of each load charge is illustrated in Table 3.

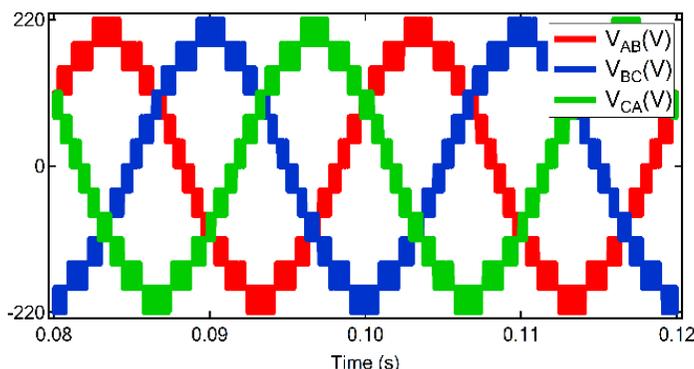


Figure 6. Simulation results of the output line-to-line voltages V_{AB} , V_{BC} , V_{CA} similar in case of highly inductive and, or highly capacitive load

The simulation results shows no effect of the charge changing on the pole or line to line voltages, but a clear effect on the phase current shape. Figures 7 and 8 indicate that the phase current in case of R-L charges shows a stable and smoother output current signal comparable to

the phase current in case of highly capacitive load and it is due to the automatic filtering of the harmonic components by the inductance.

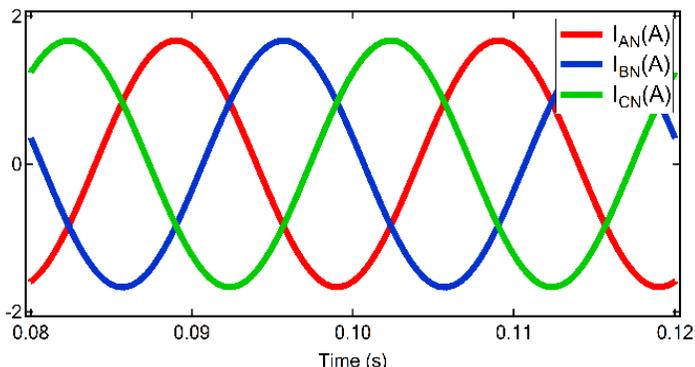


Figure 7. Simulation results of the output phase currents in case of highly inductive load ($R=20 \Omega$, $X_L=62.8 \Omega$)

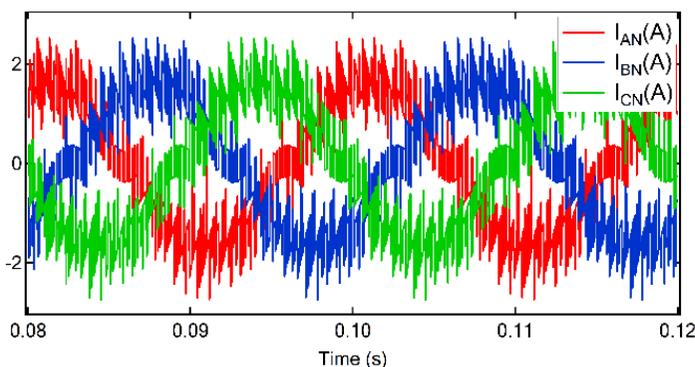


Figure 8. Simulation results of the output phase currents in case of highly capacitive load ($R=20 \Omega$, $X_C=62.8 \Omega$)

Moreover, Figure 9 shown the FFT signal for the line-to-line output voltages of the seven-level NPC, and the THD is found to be 18.30%.

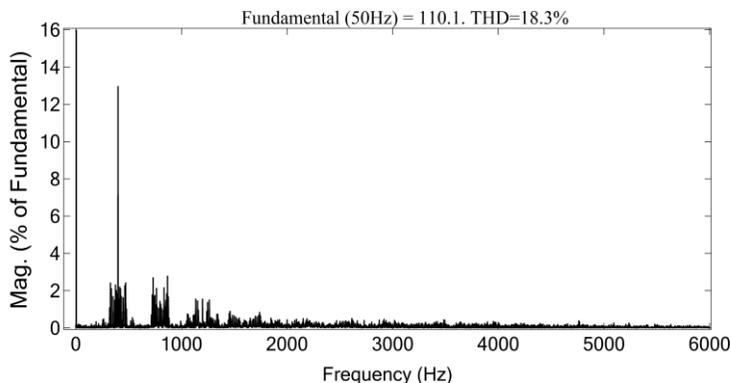


Figure 9. Simulation results of the frequency spectrum of the output line voltage for seven-level NPC inverter

Table 4 illustrate the THD value comparison for each topology structure with different output level, increasing the number of level lead to a clear decrease of the total harmonic distortion, due to the reduction of the stress on the switches. However, the MLI cascaded structure shown the lowest THD comparable to NPC and FC topologies.

Table 4. Comparison of the effect of topology and, or output voltage level on the Total Harmonic Distortion (THD) (%)

Level	Topology		
	NPC	FC	Cascade
7	18.3	18.7	18.60
11	10.84	11.40	10.90
15	06.61	08.10	05.30
31	01.38	03.8	0.40

The number of components as shown in Table V was calculated based on Table I. Analyzing this results indicates that the cascaded structure contains the less total number of elements comparable to the other topologies, which is due to the absence of power diodes and flying capacitors for NPC and FC. Instead, it showed a higher number of power sources, which can be taken as an advantage leading to limit the stress on the switches and decrease the THD.

Table 5. Total Number of components dependency on the variation of the inverter topology and, or output voltage level

Level	Topology		
	NPC	FC	Cascade
7	108	90	81
11	184	150	135
15	260	210	189
31	564	450	405

The cost-efficiency factor, which describes the relationship between the numbers of the voltage level (Components) with the value of THD as shown in Figure 10, is calculated by normalizing the (Components Number /THD) by the highest factor value calculated. The cascaded MLI structure shows an increased cost efficiency factor when increasing the number of level due to the lower components number and higher THD value comparable with other structures such NPC and FC.

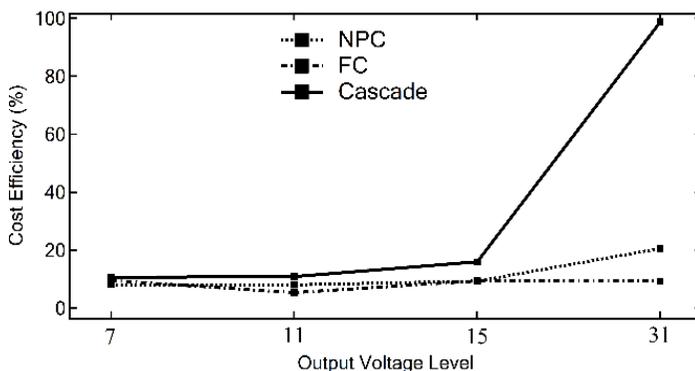


Figure 10. Cost-efficiency factor dependency on the inverter topology and, or output voltage level

4. Conclusion

The direct comparison of the three main topologies of the multilevel inverters is discussed. The point of comparison included the number of components and the total harmonic distortion relation to the increase of the inverter voltage levels. The SPWM was applied for controlling the different MLI topology and shown a simplified control and higher performance stability of the inverter toward feeding different loads.

A cost-efficiency factor is deduced combining the number of components used in each topology and each output voltage level with the value of the corresponding THD of the line-to-line voltages. The cascaded MLI inverter compared with the other two topologies gains many merits such as expressing a higher THD and a lower number of components and raise the cost-efficiency factor despite increasing the voltage levels. Moreover, the Cascaded structure does not require any capacitors or power diodes which is suitable for different voltage applications.

5. References

- [1]. O. A. El Bassiouny, S.V. Dhople, A. Davoudi, and P. L. Chapman, "Energy efficient cost-effective inverter configuration for residential photovoltaic systems", *Photovoltaic Specialists Conference (PVSC), 2010 35th IEEE*, vol., no., pp. 000400-000406, 20-25 June 2010.
- [2]. M. Orabi, A. Salem, E. Ahmed, M. Ahmed, "Study and Analysis of New Three-phase Modular Multi-Level Inverter", *IEEE Transactions on Industrial Electronics*, DOI 10.1109/TIE.2016.2547914.
- [3]. M. Ciobotaru, R. Teodorescu and F. Blaabjerg, "Control of single-stage single-phase PV inverter", *Proc. PELINCEC*, 2005.
- [4]. M. Thirumalai, V. Prakash, "Design and implementation of hybrid multilevel inverter for high output efficiency. In *Smart Structures and Systems (ICSSS), 2013 IEEE International Conference on 2013 Mar 28 (pp. 41-45). IEEE*.
- [5]. P. M. Bhagwat and V. R. Stefanovic, "Generalized structure of a multilevel PWM inverter", *IEEE Trans. Ind. Applicat.*, vol. 19, no. 6, pp. 1057-1069, 1983
- [6]. V. G. Agelidis, D. M. Baker, W. B. Lawrance and C. V. Nayar, "A multilevel PWM inverter topology for photovoltaic applications", *Proc. IEEE ISIE*, pp. 589-594, 1997
- [7]. A. Fereidouni and M. A. Masoum, "Space- vector hysteresis modulation for neutral-diode-clamped inverter in active power filter applications", *In Power Engineering Conference (AUPEC), 2015 Australasian Universities 2015 Sep 27 (pp. 1-5). IEEE*.
- [8]. J. Rodriguez, J.S. Lai, and F.Z. Peng, "Multilevel inverter: a survey of topologies, controls, and applications", *IEEE Trans Ind Electron* 2002; 49(4):724–38.
- [9]. Z. Du , L. M. Tolbert , J. N. Chiasson and B. Ozpineci, "A cascade multilevel inverter using a single DC source", *Proc. 21st Annu. IEEE APEC*, pp. 426-430, 2006
- [10]. S. Kouro, J. I. Leon, D. Vinnikov and L. G. Franquelo, "Grid-Connected Photovoltaic Systems: An Overview of Recent Research and Emerging PV Converter Technology", *IEEE Industrial Electronics Magazine*, vol. 9, pp. 47-61, 2015
- [11]. Salem, E.M. Ahmed, M. Orabi, and M. Ahmed, "New Three-Phase Symmetrical Multilevel Voltage Source Inverter. Emerging and Selected Topics in Circuits and Systems", *IEEE Journal on*. 2015 Sep; 5(3):430-42.
- [12]. V. Sonti, S. Jain, and V. Agarwal, "A new low cost and high efficiency cascaded half-bridge multilevel inverter with reduced number of switches", *In Power Electronics, Drives and Energy Systems (PEDES), 2014 IEEE International Conference on 2014 Dec 16 (pp. 1-6). IEEE*.
- [13]. S.N. Rao, D.A. Kumar, and C.S. Babu, "New multilevel inverter topology with reduced number of switches using advanced modulation strategies", *In Power, Energy and Control (ICPEC), 2013 International Conference on 2013 Feb 6 (pp. 693-699). IEEE*.
- [14]. M. Saeedifard, R. Iravani, and J. Pou, "Analysis, and control of DC-capacitor-voltage-drift phenomenon of a passive front-end five-level converter", *IEEE Trans Ind Electron* 2007; 54(6):3255–66.

- [15]. K. El-Naggar and T. H. Abdelhamid, "Selective harmonic elimination of new family of multilevel inverters using genetic algorithms", *Energy Convers Manage* 2008; 49(1):89–95.
- [16]. K. Kaviani, S.H. Fathi, N. Farokhnia, and A.J. Ardakani, "PSO, an effective tool for harmonics elimination and optimization in multi-level inverters" *In Proc 4th IEEE ICIEA*; May 25–27, 2009. P2902.
- [17]. L.G. Franquelo, J. Napoles, R.C.P. Guisado, J. I. Leon, and M.A. Aguirre, "A flexible selective harmonic mitigation technique to meet grid codes in three-level PWM converters", *IEEE Trans Ind Electron* 2007;54(6):3022–9.
- [18]. M.S. Rajan and R. Seyezhai, "Comparative study of multicarrier pwm techniques for a modular multilevel inverter", *International Journal of Engineering and Technology (IJET)*. 2013 Dec; 5(6):4850-65.
- [19]. Y. Sahali and M. K. Fellah, "A new approach for the symmetrical multilevel inverters controls optimal minimization of the total harmonic distortion (OMTHD technique)", *In Proc IEEE ISIE, Ajaccio, France*, May 4–7, 2004.
- [20]. S.R. Pulikanti, G. Konstantinou, and V.G. Agelidis, "Hybrid seven-level cascaded active neutral point clamped based multilevel converter under SHE-PWM," *IEEE Trans. Ind. Electron.*, vol. 60, no.11, pp. 4794-4805, Nov. 2013.
- [21]. A. Rufer, M. Veenstra, and K. Gopakumar, "Asymmetric Multilevel converter for high-resolution voltage phasor generation," in *Proc. EPE*, 1999, Lausanne.
- [22]. Ruderman and S. Schlosberg, "A hybrid asymmetric cascaded multilevel inverter comprising high resolution and symmetric low resolution parts", in *Electrical and Electronics Engineers in Israel*, 2008. *IEEEI 2008. IEEE 25th Convention of 2008 Dec 3* (pp. 021-025). IEEE.
- [23]. S. Laali, K. Abbaszades and H. Lesani, "A new algorithm to determine the magnitudes of dc voltage sources in asymmetrical cascaded multilevel converters capable of using charge balance control methods," in *Proc. ICEMS, 2010, Incheon, Korea*, pp. 56-61.
- [24]. S. Ranjan, S.K. Mishra, "Analysis of asymmetrical cascaded multilevel inverter for traction systems", in *Energy Efficient Technologies for Sustainability (ICEETS), 2013 International Conference on 2013 Apr 10* (pp. 708-713). IEEE.
- [25]. J. Ebrahimi, E. Babaei, and G.B. Gharehpetian, "A new topology of cascaded multilevel converters with reduced number of components for High-voltage applications," *IEEE Trans. Power Electron.*, vol.26, no. 11, pp. 3109-3118, Nov. 2011.
- [26]. E. Babaei and S.H. Hossein, "Charge balance control methods for asymmetrical cascade multilevel converters", *In Electrical Machines and Systems, 2007. ICEMS. International Conference on 2007 Oct 8* (pp. 74-79). IEEE.
- [27]. S. Boobalan and R. Dhanasekaran, "Hybrid topology of asymmetric cascaded multilevel inverter with renewable energy sources", in *Advanced Communication Control and Computing Technologies (ICACCCT), 2014 International Conference on 2014 May 8* (pp. 1046-1051). IEEE.
- [28]. S. Lu, S. Mariéthoz and K. A. Corzine, "Asymmetrical cascade multilevel converters with noninteger or dynamically changing dc voltage ratios: Concepts and modulation techniques", in *IEEE Industrial Electronics Transactions on*. 2010 Jul; 57(7):2411-8.
- [29]. F. Carnielutti and H. Pinheiro, "New modulation strategy for asymmetrical cascaded multilevel converters under fault conditions", in *Industrial Electronics Society, IECON 2013-39th Annual Conference of the IEEE 2013 Nov 10* (pp. 1074-1079). IEEE.
- [30]. F. Carnielutti and H. Pinheiro, "Hybrid modulation for asymmetrical cascaded multilevel converters under fault conditions", in *Power Electronics Conference (COBEP), 2013 Brazilian 2013 Oct 27* (pp. 155-160). IEEE.
- [31]. F. Carnielutti, H. Pinheiro, and C. Rech, "Space vector modulation for asymmetrical cascaded multilevel converters", in *Power Electronics Conference (COBEP), 2011 Brazilian 2011 Sep 11* (pp. 238-243). IEEE.

- [32]. P. McGrath, and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters", *IEEE Trans. Ind. Electron.*, vol.49, no.4, pp.858-867, Aug. 2002.



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