



Switched-Current Techniques: An Overview of Cumulative SI-Related Errors on Dynamic and Static Performances of 2nd Order LP- $\Sigma\Delta$ Ms

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Abstract: We present in this work a systematic analysis to identify Sigma Delta Modulators ($\Sigma\Delta$ Ms) non-idealities, such as charge injection error, Input/Output conductance ratio error and settling time error. A physical mechanism behind Switched Current (SI) errors is proposed. In the first time, errors mentioned above are treated separately and a behavioural model of SI cell is derived for each non-ideality. In the second time, we propose a behavioural model of Non-inverting Lossless Integrator. For typical variations of SI-related errors, simulations have been made using Matlab/Simulink. Finally we present their influences on both dynamic and static performances of the 2nd order SI Low Pass $\Sigma\Delta$ Ms (SI-LP $\Sigma\Delta$ Ms).

Keywords: Analog/Digital Converter, Switched Current technique, Sigma-Delta Modulator, error mechanisms, Dynamic and Static Performances.

1. Introduction

The staggering scaling-down of Complementary Metal Oxide Semiconductor (CMOS) Very-Large-Scale Integration (VLSI) technologies and the tendency towards Systems On Chip (SOC) are prompting the development of new digital telecommunication devices spanning the portable gadgets of nowadays (cellular phone, smart phone, tablet computer...). SI technique has been adopted in many applications (e.g. filtering [1, 2], current differentiation [3], Sigma Delta modulation [4], Digital to Analog Converters (DACs) and Analog to Digital Converters (ADCs) [5, 6, 7, 8]). $\Sigma\Delta$ Ms are very suited to implement high-resolution and robust (lower sensitivity to circuitry imperfections) ADCs, not only by increasing the oversampling ratio (a sampling frequency much larger than the Nyquist frequency) but also by pushing the quantization noise out of the band of interest. Furthermore, oversampled SI $\Sigma\Delta$ Ms have gained much popularity for their high-speed, low consumption and low supply voltage compared to the Switched-Capacitor (SC) technique [9, 10, 11, 12]. The use of such technique facilitates the integration of a whole system into a mixed signal chip. The analog portion of these chips must feature the required analog performance level in VLSI standard, what has motivated exploring analog design technique compatible with CMOS process [13, 14, 15].

Several works have been focused on identifying and modeling non-idealities in both SI and SC techniques in order to get a behavioural model of these cells. The non-ideal behavioural model has been made only at memory cell level [2, 9, 22, 23, 24]. N. Khitouni et al. and M. Loulou et al. respectively [16] and [17], have developed a mathematical model of charge injection phenomena. By using a continuous and physical formulation based on the Enz-Krummenacher-Vittoz model (EKV), A. Dei et al. [18] have developed a compact behavioural model of the MOS analogue switch for charge injection analysis. According to W. Ming Koe et al. [19], a better understanding of non-idealities in switched-capacitor circuits on sigma-delta modulators can be achieved if each of these non-idealities is studied separately.

In this work, we will study the cumulative effect of SI-related error on dynamic and static SI-LP $\Sigma\Delta$ M performances. The analysis will be focused on 1-bit 2nd-LP $\Sigma\Delta$ M. This modulator

