Power Efficient Design of Semi-Dynamic Master-Slave Single-Edge-Triggered Flip-Flop

Imran Ahmed Khan[1] and Mirza Tariq Beg[2]

[1]Department of EIE/ICE, Galgotias College of Engineering and Technology, Gr. Noida, India
[2]Department of Electronics and Communication Engg. Jamia Millia Islamia New Delhi-25, India
[1]imran.vlsi@gmail.com, [2]mtbegjamia@yahoo.co.in

Abstract: In this work, eight existing master slave single-edge-triggered flip-flops have been analyzed in 130nm process node. A new master slave single-edge-triggered flip-flop has also been proposed. The proposed flip-flop is compared with the existing flip-flops on the basis of power consumption, propagation delay and power delay product (PDP). Special emphasis has been given to power consumption. The power performance of all flip-flops as a function of supply voltage, clock frequency and data activity has been observed. TSpice results of power consumption show that the proposed flip-flop design excels rival designs for all supply voltages; all clock frequencies and all data patterns. Thus the proposed flip-flop is most power efficient flip-flop. This flip-flop also shows the third shortest delay and the second lowest PDP among all discussed flip-flops. The proposed flip-flop is best suitable for systems where low power and low area is of primary interest within a certain timing budget.

Keywords: VLSI, Latency, Low power design, Critical path, PDP.

1. Introduction

In recent years, power is emerging as the most important issue in system-on-chip (SoC) design. As the power density rises at an alarming rate, power management is becoming an increasingly critical issue for every stage of design. There are several reasons for employing low-power dissipation techniques in modern VLSI design and the most important factor is growth of the portable devices [1], [2]. The market for battery-operated devices will increase in the coming future and enhancing the battery life is an important issue. Unless low-power design techniques are applied at different levels, the portable devices will suffer from either short battery life or bulky battery pack [3]. Scaling of transistor size not only increases performance but the power density also increases substantially. So, the need for power-efficient systems has grown due to higher integration density [4].

The packaging and cooling cost of the high performance devices is becoming prohibitive. If power consumption of chip increases, the need of costly packaging and cooling techniques increases [5]. High power dissipation of a SoC will increase system-cost and also affect lifetime and reliability of system. Thus, minimizing power dissipation increases lifetime and reliability of the circuit with reduction in system cost [6]. In digital CMOS circuits, major sources of power consumption are:

1. Switching power
2. Short circuit power
3. Leakage power

The average power is given by equation (1):

$$P = p_t\left(C_L.{V_{DD}}^2.f\right) + I_{SC}.V_{DD} + I_{Leak}.V_{DD} \quad (1)$$

where

p_t = Activity factor, C_L = Effective switched loading capacitance, f = Clock frequency,
V_{DD} = Supply voltage,
I_{SC} = Short circuit current and I_{Leak} = Leakage current

The switching component of power is represented by first term of equation (1). The short circuit power is exhibited by the second part of the equation. When NMOS and PMOS transistor

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networks are on simultaneously, there is short circuit current (*Isc*) from V_{DD} to ground. Third part of equation (1) represents leakage power. Leakage current I_{Leak} may be due to substrate injection, gate leakage and sub threshold effects. This current is mainly determined by CMOS fabrication process and modelled based on its characterization [7].

The flip-flops are edge-triggered storage elements that store 1 bit of information. If the flip-flop gives output in 0 to 1 clock transition (rising edge) then the flip-flop is said to be positive edge-triggered flip-flop. If the flip-flop gives the output in 1 to 0 clock transition (falling edge) then the flip-flop is said to be negative edge-triggered flip-flop. Flip-flops and latches are exhaustively analysed circuits because these elements have a strong influence on cycle time and power consumption in synchronous circuits [8]-[11]. Clock distribution network and flip-flop which are included by clock system are the components which consume the highest power that is up to 60% of the total system power [12]. So, flip-flop designing is very important for minimum power, delay and area. Many power efficient flip-flops have been introduced so far. Some of these architectures have large transistors count leading to large area. So these are not very suitable for small, cost-efficient systems. In this work, eight existing flip-flop architectures have been extensively studied and a new Power Efficient Semi-Dynamic Flip-Flop (SDFF) has been proposed.

This paper has five sections. Conventional single-edge-triggered flip-flops are compared in Section 2. Section 3 exhibits nominal conditions of simulation. In section 4, a new design is proposed and results are also presented and performance for new design and conventional designs are compared in terms of power consumption, speed, PDP and transistor count. Section 5 ends the paper with conclusion.

2. Comparison of Conventional Designs

The conventional Transmission Gate Flip-Flop (TGFF) is given in [13]. There are sixteen transistors in TGFF. For performance improvement of a TGFF, an insertion of Transmission Gate (TG) and inverter is proposed in Push Pull Flip-Flop (PPFF) [14] between the output of master section and output of the slave section to produce a push–pull effect at the slave section, this leads to increment of four transistors. To make up this increased transistor count, two TGs are eliminated in PPFF from the feedback paths of conventional TGFF. So, PPFF also has sixteen transistors. In semi-static Pass Flip-Flop (Pass FF), the number of transistors is lowered to decrease power consumption [15]. As compared to TGFF, four transistors of feedback are replaced by single PMOS transistor. So, total transistors of pass FF became ten. As compared to Pass FF, a PMOS transistor was inserted in the feedback path in semi-static Pass Isolation Flip-Flop (PIFF) leading to activation of feedback only during OFF cycle of clock [15]. Due to this addition, the transistors count of PIFF becomes twelve however this diminishes short circuit current during ON cycle and delay as compared to Pass FF.

Low Power Master-Slave Flip-Flop (LPMSFF) is a modification of the pass FF [16]. The feedback PMOS of Pass flip-flop's master latch is removed and in slave latch a PMOS with complemented clock signal and an inverter are used to enable feedback only during OFF cycle. This leads to reduction of short circuit current during ON cycle as compare to Pass FF. There are eleven transistors in LPMSFF. For reduction in area as compared to TGFF, the two feedback TGs are removed in Low Area Flip-Flop (LAFF) [17]. This reduces the total number of transistors of LAFF to twelve. In Area Efficient Flip-Flop (AEFF), feedback of master latch is removed and in slave latch, feedback consists of a TG and an inverter [18]. There are ten transistors in AEFF. In High Performance Flip Flop (HPFF), a PMOS transistor is connected between the output of slave latch to a specific node in the master latch to provide feedback leading to lesser transistor count [19]. The static C^2MOS Flip-Flop consists of a C^2MOS feedback at the outputs of the master and the slave latches [20]. C^2MOSFF has twenty transistors leading to the largest area.

3. Simulation Conditions

To simulate the circuits, TSpice has been used. Table 1 shows the simulation parameters used for comparison. The dynamic power differs with switching activities. So, for fair comparison of power of the circuits, several data patterns must be applied with varying activity rates [21]. Therefore in this paper, six data patterns have been applied at the input for comparison of power consumption of different architectures:

0000000000000000
1111111111111111
1100110011001100
1010101010101010
1111010110010000
0100000000000000

Table 1. CMOS Simulation parameters

Parameter	Value	Parameter	Value
CMOS Technology	130 nm	Temperature	25° C
MOSFET Model	BSIM 3v3 level 53	Duty Cycle	50 %
Max. Gate Width	1.04 µm	Nominal Clock Frequency	400MHz
Min. Gate Width	0.26 µm	Nominal Supply Voltage	1.6V
Rise Time of Clock & Data	100 ps	Nominal Data Sequence	11110101 10010000
Fall Time of Clock & Data	100 ps		

Propagation delay increases on optimizing a circuit for power consumption and vice versa. The designs have been simulated to attain minimum power consumption. To reduce power consumption and area, the width of transistors that are located along non critical path is kept minimum in all flip-flops.

4. Proposed Power Efficient Semi-dynamic Flip-Flop

In the proposed flip-flop, an NMOS pass transistor is used in place of TG in master latch to reduce number of transistors. This reduces area and power of the circuit. However, in slave section of the circuit, TG is used to overcome disadvantage of pass transistor i.e. to make the output signal clean and stable. In the proposed negative edge triggered Semi-Dynamic Flip-Flop (SDFF shown in Figure 1), two weak PMOSFETs are applied in series to provide feedback. The gate of one PMOS is connected to the ground that leads to permanently 'ON' transistor which reduces switched capacitance. SDFF uses only eleven transistors among them three are clocked transistors. This flip-flop has the lowest number of clocked transistors among all the discussed flip-flops.

The clock load capacitance decreases with decrease in number of clocked transistors that result in reduced power consumption in the clock distribution network [22]. Generally clock has the highest switching activity. Hence by lowering the number of clocked transistors, power consumption of the proposed SDFF is further reduced.

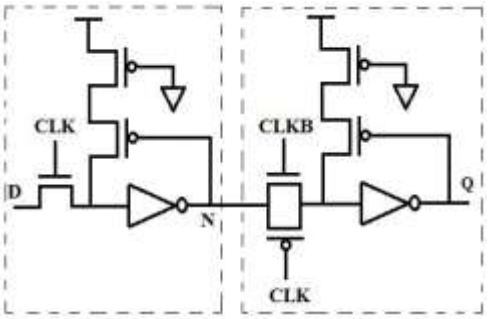

Figure 1. Proposed Power Efficient Semi-Dynamic Flip-Flop (SDFF)

Table 2 shows power consumption with variation of supply voltage. Power increases with increase in supply voltage because switching power, short circuit power and leakage power depend on supply voltage and the switching power is proportional to square of the supply voltage. Approximately 90% power dissipation in CMOS logic is due to the dynamic (switching) power [23]. So power dissipation rapidly reduces with reduction in the supply voltage. The proposed SDFF consumes lesser power as compared to other existing flip-flops for all supply voltages. LAFF failed at 1.2V, 1.3V and 1.4V. The average is taken for fair comparison; the results show that SDFF consumes 52.08%, 46.91%, 56.37%, 18.44% 65.19%, 57.72%, 41.29%, and 54.04% lesser power than existing flip-flops respectively. Figure 2 gives a consolidated graphical representation of power consumption as a function of supply voltage. It can be observed from the figure that the proposed SDFF consumes the lowest power for all supply voltages. The LPMSFF consumes the second lowest power for all supply voltages. At 1.2V, 1.3V and 1.4V existing C^{2}MOSFF consumes the highest power. At 1.6V LAFF consumes the highest power. While at 1.8V and 2V AEFF consumes the highest power.

Table 2. Power consumption in µW with variation of supply voltage for 400MHz clock frequency and 1111010110010000 data pattern

VDD	**1.2V (µW)**	**1.3V (µW)**	**1.4V (µW)**	**1.6V (µW)**	**1.8V (µW)**	**2.0V (µW)**	**Avg. Power (µW)**
PPFF	4.8	5.65	6.5	10.1	12.4	15.4	9.14
Pass FF	4.7	5.52	6.4	8.4	10.7	13.8	8.25
PIFF	4.97	5.94	7.34	10.9	13.64	17.42	10.04
LPMSFF	3.0	3.44	4.1	5.2	6.9	9.6	5.37
LAFF	Fail	Fail	Fail	11.8	11.9	14.05	12.58
AEFF	3.83	5.00	6.31	9.67	15.05	22.3	10.36
HPFF	4.6	5.24	6.00	7.9	9.5	11.5	7.46
C^{2}MOSFF	5.4	6.30	7.4	10.1	12.9	15.1	9.53
Proposed SDFF	2.64	3.15	3.2	4.22	5.17	7.9	4.38

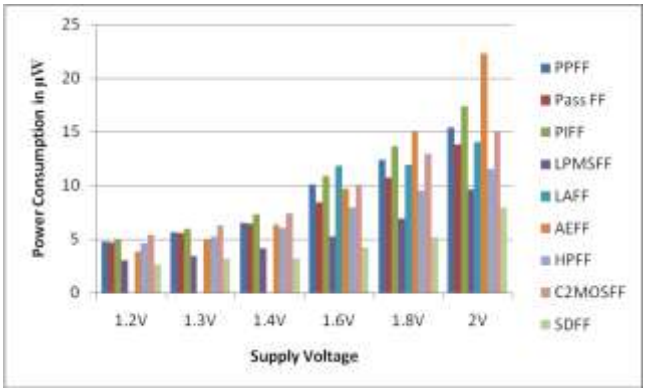

Figure 2. Power consumption in µW with variation of supply voltage

Table 3 shows power consumption in microwatts as a function of supply voltage for 400MHz clock frequency and 0100000000000000 data pattern. The proposed SDFF consumes lesser power than all existing flip-flops at all supply voltages. It can be observed from the average results that the proposed SDFF has 41.62%, 43.19%, 47.35%, 17.36% 59.38%, 28.54%, 44.68%, and 56.22% improvement in power consumption than existing flip-flops respectively. Figure 3 gives a consolidated graphical representation of power consumption for these conditions. This can be observed that proposed SDFF consumes the lowest power for all supply voltages.

LPMSFF and C^{2}MOSFF consume the second lowest and highest power respectively for all supply voltages.

Table 3. Power consumption in µW with variation of supply voltage for 400MHz clock frequency and 0100000000000000 data pattern

VDD	1.2V (µW)	1.3V (µW)	1.4V (µW)	1.6V (µW)	1.8V (µW)	2.0V (µW)	Avg Power (µW)
PPFF	3.26	3.89	4.42	6.24	7.69	9.24	5.79
Pass FF	3.54	4.18	4.82	5.98	7.52	9.64	5.95
PIFF	3.74	4.38	5.05	6.88	8.22	10.24	6.42
LPMSFF	2.48	2.7	3.19	4.09	5.31	6.79	4.09
LAFF	Fail	Fail	Fail	7.82	7.73	9.41	8.32
AEFF	2.67	3.02	3.54	4.89	6.24	8.01	4.73
HPFF	3.95	4.32	4.98	6.48	7.56	9.39	6.11
C^{2}MOSFF	4.54	5.31	6.18	8.02	10.27	11.98	7.72
Proposed SDFF	2.07	2.42	2.55	3.41	4.58	5.25	3.38

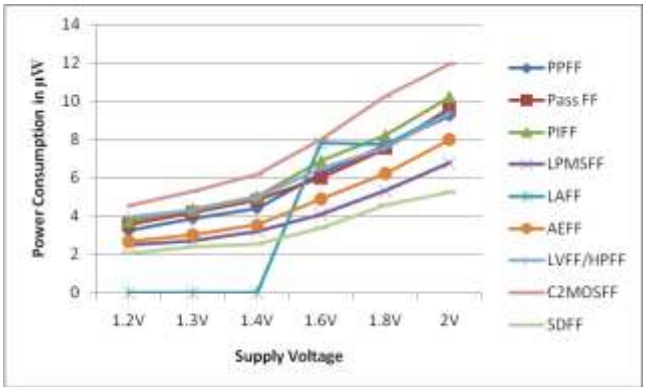

Figure 3. Power consumption with variation of supply voltage for 0100000000000000 data pattern

Table 4. Power consumption in µW with variation of clock frequency

Clock Frequency	100MHz (µW)	**200MHz (µW)**	**250MHz (µW)**	**400MHz (µW)**	**1000 MHz (µW)**	**Avg Power (µW)**
PPFF	6.16	7.09	8.36	10.1	15.42	9.43
Pass FF	5.1	6.66	5.79	8.4	15.92	8.37
PIFF	7.11	10.17	8.34	10.9	16.78	10.66
LPMSFF	2.27	3.11	3.64	5.2	10.16	4.88
LAFF	8.77	9.74	9.21	11.8	18.28	11.56
AEFF	6.78	7.8	8.23	9.67	15.37	9.57
HPFF	2.43	3.61	4.22	6.48	13.25	5.88
C^{2}MOSFF	4.80	6.19	6.96	10.1	19.26	9.46
Proposed SDFF	2.32	3.11	3.32	4.22	8.69	4.33

Table 4 shows power Vs clock frequency. The power increases with increase in clock frequency. The proposed SDFF consumes smaller power as compared to all other discussed circuits for all clock frequencies apart from 100MHz. SDFF consumes second smallest power at 100MHz. The average results show that the proposed SDFF has 54.08%, 48.27%, 59.38%, 11.27%, 62.54%, 54.75%, 26.36% and 54.23% lesser power consumption than existing flip-flops respectively. It can be observed from figure 4 that the proposed SDFF consumes the smallest power for all clock frequencies apart from 100MHz. At 100MHz, LPMSFF consumes the lowest

power while for other clock frequencies the flip-flop has the second lowest power. LAFF consumes the highest power for all clock frequencies apart from 200MHz and 1GHz. For these frequencies PIFF and C^{2}MOSFF consumes the highest power respectively.

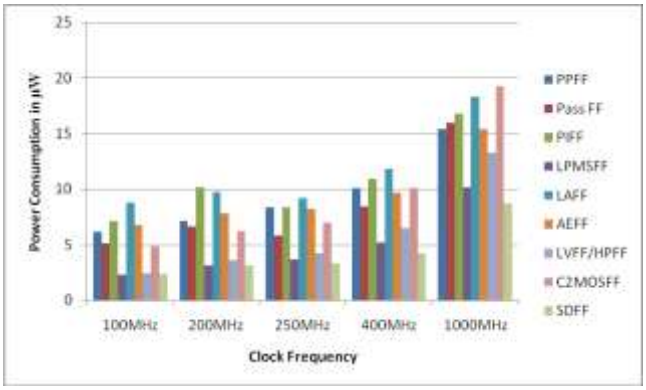

Figure 4. Power consumption with variation of clock frequency

Table 5. Power consumption in µW with variation of data activity

Data activity	111111 11111 11111	000000 00000 00000	111101 01100 10000	110011 00110 01100	101010 10101 01010	010000 00000 00000	Avg Power (µW)
PPFF	4.92	5.14	10.1	9.89	15.22	6.24	8.59
Pass FF	4.76	5.18	8.37	8.67	12.79	5.89	7.61
PIFF	5.21	5.82	10.9	10.78	16.23	6.88	9.3
LPMSFF	3.71	3.84	5.2	5.05	6.47	4.09	4.73
LAFF	4.40	4.49	11.8	11.61	18.72	7.82	9.81
AEFF	3.88	9.37	9.67	9.60	11.89	4.89	8.22
HPFF	5.95	6.23	7.91	7.75	9.82	6.48	7.36
C^{2}MOSFF	7.14	6.53	10.08	9.60	13.69	8.02	9.18
Proposed SDFF	2.86	2.6	4.22	4.36	6.17	3.41	3.94

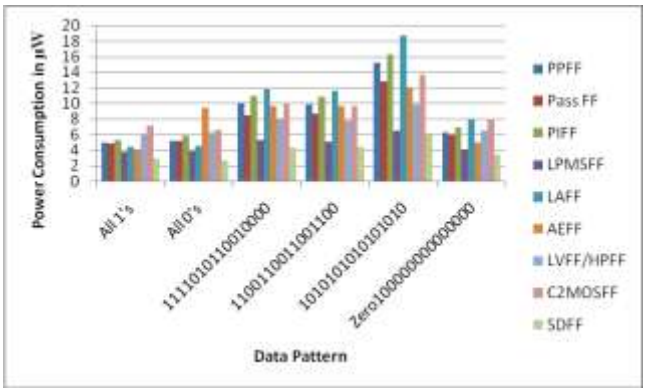

Figure 5. Power consumption for various data activities

Table 5 shows power consumption in microwatts for various data activities. The proposed SDFF consumes smaller power as compared to all other discussed circuits for all data activities The average results indicate that the proposed SDFF has 54.13%, 48.23%, 57.63%, 16.70% 59.84%, 52.07%, 46.47% and 57.08% improvement in power consumption over existing flip-flops respectively. Power consumption for various data activities is represented by Figure 5. It

can be observed from the figure that for all data activities, SDFF consumes the lowest power and LPMSFF consumes the second lowest power among all the discussed flip-flops.

Table 6. Delay in pS with variation of supply voltage

VDD	1.2V (pS)	1.3V (pS)	1.4V (pS)	1.6V (pS)	1.8V (pS)	2.0V (pS)	Avg Delay (pS)
PPFF	137.85	99.99	116.4	132.4	111.75	95.3	115.62
Pass FF	133.6	79.77	103.6	100.3	81.3	66.15	94.11
PIFF	126.65	63.78	43.52	9.9	78.61	69.54	65.33
LPMSFF	86.6	39.47	72.75	6.65	46.35	43.25	49.18
LAFF	Fail	Fail	Fail	285.36	157.31	114.19	185.62
AEFF	593.2	293.43	193.65	98.25	58.4	43.75	213.45
HPFF	119.95	74.31	56.35	41.25	34.05	30.3	59.37
C^2MOSFF	41.35	25.61	18.25	13.35	11.55	10.3	20.07
Proposed SDFF	112.97	135.99	7.03	5.08	4.22	41.16	51.08

Table 6 demonstrates CLK-to-Q delay with variation of supply voltage. The proposed SDFF has shorter delay as compared to other circuits except LPMSFF and C^2MOSFF. The proposed SDFF has the shortest delay at 1.4V, 1.6V and 1.8V. C^2MOSFF has the shortest delay at 1.2V, 1.3V and 2V and the second shortest delay at 1.4V and 1.8V. LPMSFF has the second shortest delay at 1.2V, 1.3V and 1.6V, while HPFF has the second shortest delay at 2V supply voltages. LAFF failed at 1.2V, 1.3V and 1.4V and has the longest delay at remaining supply voltages. AEFF has the longest delay at 1.2V, 1.3V and 1.4V. The average results show that SDFF has 55.82%, 45.72%, 21.81%, 72.48%, 76.07% and 13.96% improvement in delay over existing flip-flops respectively except LPMSFF and C^2MOSFF. However the flip-flop has 3.72% and 60.71% longer delay than the two mentioned flip-flops. Table 7 shows PDP (fJ) with variation of supply voltage for 0100000000000000 data pattern. The simulation results illustrate that the proposed *SDFF* has lesser PDP as compared to other circuits except *C^2MOSFF*. The proposed SDFF has the lowest PDP at 1.4V, 1.6V and 1.8V and the second lowest PDP at 2V. C^2MOSFF has the lowest PDP at 1.2V and 2V and the second lowest PDP at 1.3V, 1.4V and 1.8V. LPMSFF has the lowest PDP at 1.3V supply voltage the second lowest PDP at 1.2V and 1.6V. LAFF failed at 1.2V, 1.3V and 1.4V and has the highest PDP at remaining supply voltages. AEFF has the highest PDP at 1.2V, 1.3V and 1.4V. The proposed SDFF has 78.83%, 71.18%, 65.89%, 15.28%, 90.42%, 89.88% and 49.49% lesser PDP respectively except C^2MOSFF, this flip-flop has 14.51% lesser PDP than SDFF.

Table 7. PDP (fJ) with variation of supply voltage

VDD	1.2V (fJ)	1.3V (fJ)	1.4V (fJ)	1.6V (fJ)	1.8V (fJ)	2.0V (fJ)	Avg PDP (fJ)
PPFF	661.68	564.94	756.60	1337.24	1385.70	1467.62	1056.77
Pass FF	627.92	440.33	663.04	842.52	869.91	912.87	776.41
PIFF	629.45	378.85	319.44	107.91	1072.24	1211.39	655.91
LPMSFF	259.80	135.78	298.28	34.58	319.82	415.20	264.10
LAFF	Fail	Fail	Fail	3367.25	1871.99	1604.37	2335.10
AEFF	2271.96	1467.15	1221.93	950.08	878.92	975.63	2211.34
HPFF	551.77	389.38	338.10	325.88	323.48	348.45	442.90
C^2MOSFF	223.29	161.34	135.05	134.84	149.0	155.53	191.27
Proposed SDFF	298.24	428.37	22.50	21.44	21.82	325.16	223.73

Table 8 compares the average power for each circuit with variation of supply voltage. These values are expressed in microwatts for all zeros data pattern and 400MHz clock frequency. The proposed SDFF consumes lesser power than existing flip-flops for all supply voltages. SDFF has 37.92%, 42.62%, 45.95%, 20.68%, 50.27%, 24.12%, 50.09% and 59.12% improvement in

power performance as compared to discussed circuits respectively. In Figure 6 average power consumption is represented as a function of supply voltage for all zeros input data pattern. Proposed SDFF consumes the lowest power at all supply voltages. LPMSFF has the second lowest power consumption and C^2MOSFF has the highest power consumption for all supply voltages.

Table 8. Power consumption with variation of supply voltage for all 0's data pattern

VDD	1.2V (µW)	1.3V (µW)	1.4V (µW)	1.6V (µW)	1.8V (µW)	2.0V (µW)	Avg Power (µW)
PPFF	2.59	3.2	3.61	4.92	5.84	6.88	4.51
Pass FF	3.01	3.5	3.98	4.76	6.03	8.01	4.88
PIFF	3.11	3.64	4.22	5.21	6.37	8.51	5.18
LPMSFF	2.3	2.4	2.74	3.71	4.55	5.45	3.53
LAFF	Fail	Fail	4.04	4.40	6.36	7.73	5.63
AEFF	2.35	2.58	2.96	3.88	4.63	5.73	3.69
HPFF	3.70	4	4.54	5.95	6.89	8.56	5.61
C^2MOSFF	4.10	4.80	5.54	7.14	9.11	10.41	6.85
Proposed SDFF	1.74	2.05	2.14	2.86	3.87	4.15	2.8

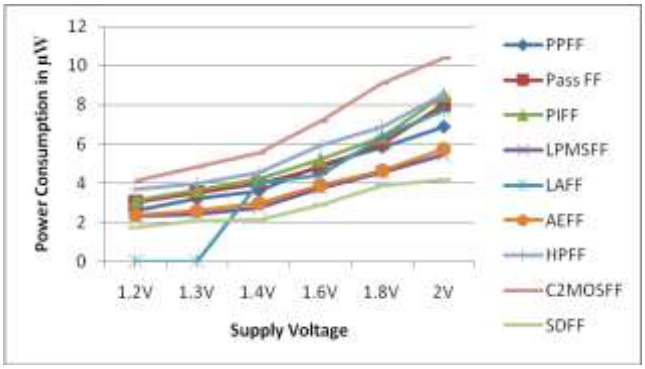

Figure 6. Power consumption with variation of supply voltage for all 0's data pattern

Table 9. Power consumption with variation of supply voltage for all 1's data pattern

VDD	1.2V (µW)	1.3V (µW)	1.4V (µW)	1.6V (µW)	1.8V (µW)	2.0V (µW)	Avg Power (µW)
PPFF	2.86	3.3	3.57	5.14	6.08	7.68	4.77
Pass FF	3.06	3.6	4.17	5.18	5.47	6.73	4.70
PIFF	3.22	3.8	4.39	5.82	6.84	9.99	5.68
LPMSFF	2.15	2.5	2.88	3.84	4.91	7.7	4.00
LAFF	2.68	3.27	3.77	4.49	6.48	7.35	4.67
AEFF	3.16	4.2	5.57	9.37	16.81	23.41	10.42
HPFF	3.42	4.01	4.68	6.23	6.95	7.81	5.52
C^2MOSFF	3.68	4.3	4.96	6.53	8.29	9.76	6.25
Proposed SDFF	1.58	1.85	2.12	2.61	2.83	5.88	2.81

Table 9 presents average power for each circuit with variation of supply voltage for all 1's data pattern for all 1's data pattern. The proposed SDFF consumes lesser power than existing flip-flops for all supply voltages. The results show that the proposed SDFF has 41.09%, 40.21%, 50.53%, 29.75%, 39.83%, 73.03%, 49.09% and 55.04% improvement in power performance as compared to other circuits respectively. Figure 7 gives a consolidated graphical representation. It can be observed that the proposed SDFF consumes the lowest power for all supply voltages. The LPMSFF has the second lowest power consumption for all supply voltages except 2V; at this supply voltage Pass FF has the second lowest power consumption. At 1.2V and 1.3V

C^2MOSFF has the highest power consumption. As supply voltages increase, the power performance of AEFF degrades and at 1.4V, 1.6V, 1.8V and 2V supply voltages the flip-flop consumes the highest power.

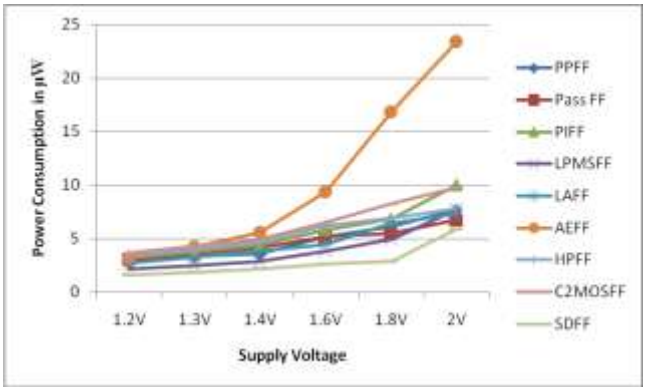

Figure 7. Power consumption with variation of supply voltage for all 1's data pattern

Table 10. Number of transistors and clocked transistors

Flip-flop	No. of Transistors	No. of clocked Transistors
PPFF	16	6
Pass FF	10	4
PIFF	12	6
LPMSFF	11	5
LAFF	12	4
AEFF	10	4
HPFF	9	5
C^2MOSFF	20	8
Proposed SDFF	11	3

Table 10 shows the number of transistors (excluding inverter to generate complemented clock signal) of all existing and proposed single-edge-triggered flip-flop architectures. It also shows the number of transistors that switches with every clock pulse, hence these transistors consumes large dynamic power. The existing HPFF requires the least number of transistors for their implementation. The existing Pass FF and AEFF have the second lowest transistor count. The proposed SDFF has the lowest number of clocked transistors. There are only three clocked transistors in this flip-flop. The existing C^2MOSFF has the largest transistor count requiring 20 transistors for its implementation. C^2MOSFF has largest area and power consumption but shows the shortest delay. Due to requirement of large number of transistors and hence area, C^2MOSFF is not suitable for small, low-cost systems.

5. Conclusion

Eight existing master slave single-edge-triggered flip-flops named PPFF, Pass FF, PIFF, LPMSFF, LAFF, AEFF, HPFF and C^2MOSFF are analyzed in this work. A new master slave single-edge-triggered architecture named SDFF has been proposed. A detailed comparison of the existing and proposed flip-flops is presented in the work. The comparison parameters taken were power consumption, propagation delay and PDP. Results suggest that the proposed flip-flop has improvement in terms of total power dissipation when compared with existing designs. For all supply voltages and all data activities, the proposed SDFF consumes the lowest power and LPMSFF consumes the second lowest power. The proposed SDFF consumes the lowest power for all clock frequencies other than 100MHz. SDFF consumes the second lowest power

at 100MHz. LPMSFF consumes the lowest power at 100MHz while for other clock frequencies this flip-flop has the second lowest power. LAFF consumes the highest power for all clock frequencies apart from 200MHz and 1GHz. For these two frequencies PIFF and C^2MOSFF consumes the highest power respectively.

AEFF has longer delays at lower supply voltages (up to 1.4V). With the increase in supply voltages, the delay of this flip-flop improves. The existing LAFF failed at 1.2V, 1.3V and 1.4V and for all other supply voltages this flip-flop has longer delays and highest PDP. Overall AEFF has the longest delay and existing C^2MOSFF has the shortest delay. The proposed SDFF has shorter delay as compared to other discussed architectures except LPMSFF and C^2MOSFF. SDFF has up to 76.07% improvement in delay. AEFF has the higher PDP for low supply voltages. The existing C^2MOSFF has the lowest PDP. The proposed SDFF has lesser PDP than all discussed architectures except C^2MOSFF and has up to 90.42% improvement in PDP.

The existing HPFF requires the least number of transistors for its implementation. The existing Pass FF and AEFF have the second lowest transistor count. SDFF has lowest number of clocked transistors. The existing C^2MOSFF has the largest transistor count requiring 20 transistors for their implementation. C^2MOSFF shows the shortest delay but this flip-flop has highest area and power consumption. Due to requirement of large number of transistors and hence area for implementation, C^2MOSFF is not suitable for small, low-cost systems. The proposed SDFF is most power efficient flip-flop for all conditions; it also has the second smallest PDP with third shortest delay among all discussed flip-flops and also occupies small area. The proposed flip-flop is best suitable for systems where low power and low area is of primary interest within a certain timing budget.

6. References

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Imran Ahmed Khan received his B.Tech. & Ph.D. degrees from Jamia Millia Islamia, India in 2006 & 2015 respectively and M.Tech. degree from CDAC-Noida, G.G.S. Indraprastha University, India in 2009. In the same year, he joined Cadence. At present, he is working as Associate Professor in A.K. Technical University, Lucknow. He has interest in designing of low power circuits. He has authored several research papers in international/national journals and conferences. He has authored and co-authored many books and book chapters.

Mirza Tariq Beg received his Ph.D. degree from Jamia Millia Islamia, India in 2003, M.Tech. from Delhi University (DU), India in 1987 and B.Tech. from AMU, Aligarh, India in 1985. He started his career as an Assistant Professor from Jamia Millia Islamia, India in 1987. At present, he is working as Professor since 2003 in the same organization. His interests include Data Communication and Computer Networks, Microwave Engineering, low power circuit design. He has authored and co-authored many papers in International/National Journals and International/National conferences.