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Optimal Reactive Power Compensation by Shunt Capacitor Sizing Using Harmony Search Algorithm in Unbalanced Radial Distribution System for Power loss Minimization

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Abstract: Electricity demand exceeds the supply leading to regional blackout. The power generated is transmitted through a large network and significant power losses in transmission and distribution feeders. Loss reduction through various methods has the potential to yield huge savings in economic growth and environmental impact. One such effective loss minimization method is to inject reactive power by placing shunt capacitors at appropriate places with proper size. A Harmony Search Algorithm methodology is proposed in this work to identify the appropriate size of shunt capacitors by taking the objective as minimizing the cost associated with real power losses along with installation cost of shunt capacitors in an unbalanced radial distribution network. The bus voltage limits, number/size of installed capacitors at each node are taken as constraints. A two stage methodology is adopted in this work to get the solution of the optimization problem. In the first stage, the voltage stability index values at each bus is computed and the node with minimum value of voltage stability index is identified as the most receptive node to voltage slump and such a node is considered as candidate node for installation of shunt capacitors. In the second stage the HSA methodology is used to ascertain the suitable capacitor size. The backward / forward sweep algorithm based Radial distribution load flow algorithm is utilized for power flow simulation. The proposed Harmony Search Algorithm is implemented on the modified IEEE 13 and 37 bus URDN.

Keywords: Backward/forward based load flow (BFLF), Unbalanced Radial Distribution Network (URDN), Harmony search algorithm (HSA), Voltage Stability Index (VSI).

1. Introduction

Distribution networks starts with single source of supply from distribution substation and ends with the individual consumer loads through radial structure of distribution feeder lines with laterals and sub laterals and it is inherently unbalanced with high R/X ratios. Due to constant increase in power demand, there is a need to upgrade the substation capacity and number of feeder/lateral lines and this leads to huge investments to the electric utilities. Instead of that, to meet out the load demand various loss minimization techniques like network reconfiguration, installation of shunt capacitors, conductor replacement, optimal change of transformer tap are proposed. Network reconfiguration cannot be the effective solution to reduce the power losses due to reactive power flows in the distribution lines during heavy reactive power load demands. But the installation of shunt capacitors to inject reactive power at optimal places with optimal size will results the reduced reactive power flows within the system resulting the reduction of power loss with improved voltage profiles.

For optimal location of shunt capacitors with proper sizing along with % THD to achieve the power loss reduction as objective has been solved by integrating Particle Swarm Optimization (HPSO) technique with harmonic power flow algorithm is proposed in [1].A heuristic numerical algorithm has been proposed for optimizing the size of shunt capacitors with distorted substation voltages with rms values of bus voltage magnitude limits and THD

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are considered as constraints in [2]. Network topology based power flow calculation for radial distribution system has been discussed in [3]. Unbalanced radial distribution network with the consideration of mutual coupling among the phases has been proposed in [4]. Identification of weak nodes in the radial distribution networks which are more possible to voltage collapse by computing voltage stability index is proposed in [6]. The shunt capacitor position and sizing problem using HSA is suggested and implemented on the IEEE 34 bus RDS in [7]. The shunt capacitor placement and network reconfiguration problems are combined together and solved via HSA to attain power loss reduction with improved bus voltage profile has been proposed in [8].

2. Mathematical Formulation

The proposed problem is mathematically formulated as nonlinear optimization problem, since the location and rating of capacitors to be placed in distribution networks are discrete in nature. Minimizing the cost associated with real power loss along with cost involved for capacitors installation are taken as the objective function and it is subjected to the following constraints.

A. Objective Function

In this proposed work, the mathematical model of the objective function can be formulated as shown below [1].

$$F = K_p Ploss + \sum_{1=1}^{nc} K_{ci} Q_{ci} \quad (\$) \tag{1}$$

Where,

K_p: Real power loss cost/year in KW

K_{ci}: Reactive power cost/year in \$ / KVAR injected by shunt capacitor at bus "i".

Q_{ci}:Total reactive power injected at i th bus (in kVAR)

nc : Total quantity of capacitors to be installed.

P_{loss}: Sum of active power losses in the U RDN.

The real power losses in URDN found by using Backward/Forward sweep based radial distribution load flow (BFLF) technique [3].The cost of shunt capacitor depends on capacitor size to be placed in load flow technique. The cost of reactive power injection by the capacitor (($/kVAR) is cheap, if the capacitor size to be installed is larger [2]. In the proposed optimization problem, the size of shunt capacitor is considered as the control variable.

Constraints:

A. Equality constraints

The Backward/Forward based load flow (BFLF) technique based on node current injection. The equality constraint is the node (or) bus current mismatch equations as it is related with the nonlinear load flow equations. It can be mathematically formulated in a vector form as,

$$g(x, u) = 0 \tag{2}$$

Where "x" and "u" are dependent variable and independent variable vectors.

B. Inequality constraints

The nominal bus voltages limits and total number of shunt capacitors to be located in the URDN are considered as inequality constraints

B.1. Bus voltage limits

During the optimization process, the rms value of bus voltages should be kept inside acceptable tolerance limits

$$V_{min} \le |V_i| \le V_{max} \tag{3}$$

Where

V_{min} : the minimum limits for bus voltage magnitude

V_{max} : the maximum limits for bus voltage magnitude

$|V_i|$: i^{th} bus voltage magnitude and it can be defined as,

$$|V_i| = \sqrt{|V_i^{(1)}|^2} \quad i = 1,2,...,n$$

"n" represents the total number of nodes in URDN.

B.2. Rating and total number of shunt capacitors

The multiple integers of the smallest size of standard capacitor commercially existing with discrete size are also taken into consideration along with the total KVAR injection by the capacitors to be placed should not exceeds the total amount of reactive power demand of the URDN be considered as one of the constraints.

$$Qci \le KQ_0, \qquad K = 1,2\ldots,nc \tag{4}$$

Where,

Q_0 : the minimum size of capacitors available.

Qci : the total KVAR injection by shunt capacitors to be installed.

nc : total quantity of capacitors to be installed

$$\sum_{i=1}^{nc} Q_{ci} \le Q_\tau \tag{5}$$

Where

Q_T : Sum of KVAR demand of the URDN.

3. Overview Of Harmony Search Algorithm (HSA)

HSA has been proposed by Geem, Kim and Loganathan [9]-[10]. It originated from the natural phenomena of music played on musical instruments. The improvisation is based on random process (or) based on musical experience of musician to attain pleasing harmony. In real world optimization problems based on the decision variables values, the objective function is evaluated and it can be improved via iterative process and finally a global solution is reached [7] as like in finding the best pleasing harmony in HSA. The HSA algorithm is successfully applied in various benchmarking problems like data mining, visual tracking, traveling salesman problems and so on. It can be used effectively by choosing correct parameters and their values within their limits. The computational procedures of HSA are given below

Step-1: Parameters initialization of HSA algorithm.
Step-2: Initialization of Harmony Memory Vector (HMV)
Step-3: Improvisation of the new Harmony Memory Vector.
Step-4: Updating the HMV.
Step-5: Repeat step 3 & 4 until the termination criteria has been met.

Step - 1 Initialize the parameters of HSA.

HSA parameters are initialized by choosing the suitable value for HM size. It is used to decide the number of solution vectors and in HM a group of decision variables are stored. The HMCR (Harmony Memory Consideration Rate) and PAR (Pitch Adjusting Rate) are utilized to get best solution vector.

Step - 2 Harmony Memory Vector initialization

In HMV, solution vectors are randomly generated are utilized to form the HMS matrix

Step - 3. Improvisation of Harmony Memory (HMV)

The following three measures are adopted to improve the New Harmony vector value [9]. The first one is Memory Consideration and second one is Pitch Adjustment and third one is Random Selection. The variable values of HM vector $x_2', x_3', \ldots x_N'$ are chosen randomly. The HMCR value is chosen between 0 and 1, and it is the rate of selecting one value from the previously stored values in the Harmony Memory Vector. (1- HMCR) is the rate of randomly choosing each value for the variable from the specified range of values as in (6),

if (rand( ) < HMCR)
$xi \leftarrow xi \in \{xi^1, xi^2, ..., x_1^{HMS}\}$
else
$xi \leftarrow xi \in Xi$
end (6)

rand ( ) is the uniform random number lies within 0,1 and "Xi" is the possible range of values for each decision variable (x_i'). HSA will select the decision variable value from values stored in the Harmony Memory with 90 % probability, if HMCR value chosen as 0.9 or from the possible range lies between (100-90) % probability [8]. Each element from the memory consideration is to be pitch adjustment as,

If (rand ( ) < PAR)
$xi' = xi' \pm BW*rand( )$
else $xi' = xi'$ (7)

Where, "BW" represents a random distance bandwidth

Step - 4. Updating Harmony Memory Vector (HMV)

A new modified and improved harmony vector values and its best fitness function values computed in step 3 are added in HM by replacing the existing worst harmony vector. Otherwise, the new generated vector value is discarded.

Step - 5: step 3 and step 4 are repetitive until the termination condition is reached.

4. Solution Methodology

To demonstrate the effectiveness of the HSA algorithm, modified IEEE 13 bus and 37 bus URDN are taken into consideration [5]. Voltage stability indices are computed at all nodes of the proposed test systems to minimize the computational burden and dimension of the resultant vector. The optimal location for placing the shunt capacitor is decided based on the minimum value of voltage stability index (VSI) computed. The structure of resultant vector contains the different KVAR values (capacitor sizes) required to be placed at weak node with minimum value of VSI.

In Harmony Memory matrix, the solution vector format is as,

HMS = [KVARi …KVARn]

The solution vector (HMS^1) is represented as

HMS^1= [Capacitor sizes in KVAR]

All feasible solution vectors are created without violating the inequality constraints by choosing the appropriate capacitor sizes in KVAR randomly from table 1.

Table 1. Standard capacitor sizes along with their annual cost/kvar

Qc (kVAR)	Kc ($/kVAR)	Qc (kVAR)	Kc ($/kVAR)
150	0.500	900	0.183
300	0.350	1050	0.228
450	0.253	1200	0.170
600	0.220	1350	0.207
750	0.276	1500	0.201

In this proposed method, the capacitor values are chosen randomly from 150 KVAR to 1500 KVAR as listed from table 1 [1] to generate initial solution vector along with its corresponding objective function values estimated from BFLF to be stored in HMS matrix is as shown below [11].

The objective function values (fitness1, fitness 2…... fitness n) stored in HM matrix is improved by removing the bad solution vectors in the subsequent iterative process. The new improved solution vectors are pitch adjusted .The worst vectors of preceding iteration will be removed with a new one chosen based on the minimum value of the objective function. This course of action is repeated until a stopping criterion is fulfilled.

$$\begin{bmatrix} 261.76 & \mathit{fitness}\ 1 \\ 168.30 & \mathit{fitness}\ 2 \\ 482.21 & \mathit{fitness}\ 3 \\ 950.64 & \mathit{fitness}\ 4 \\ \ldots & \ldots\ldots \\ \ldots & \ldots\ldots \\ 275.53 & \mathit{fitness}\ 15 \end{bmatrix}$$

5. Voltage Stability Index

The optimization problem is formulated for identification of best possible capacitor ratings and its optimal location in an URDN using Harmony Search Algorithm to achieve the goal of real power loss minimization with improved voltage profile. The VSI values of each node near to unity are the indication of the radial distribution system stable operating condition. The VSI values of all the node of proposed URDN are computed to indicate the weak buses which are prone to voltage collapse. The best location for placing shunt capacitor is identified by selecting a candidate node with minimum value of VSI among all the nodes (6).

Equation of Voltage Stability Index (VSI):

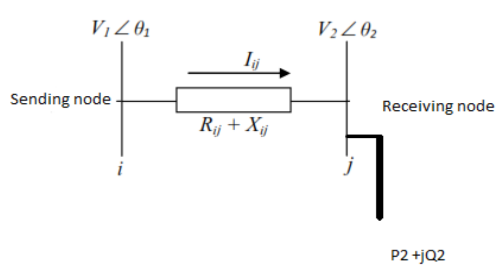

Figure 1. Branch of radial distribution network

VSI in all the nodes of the URDN are computed as follows,

From figure 1, the branch current "Iij" between the sending node "i" and the receiving node "j", can be calculated as,

$$Iij = (V_1 - V_2) / (Rij + jXij) \quad (8)$$

$$[P\text{-}jQ] = (V2 * Iij) \quad (9)$$

Where,

i, j - Sending and receiving end nodes of a branch in URDN

P, Q - The real and reactive power load at bus j

V_1, V_2 - "i" th node and "j" th nodes voltage magnitudes

The VSI of node "j" is computed using the following equations as,

$$VSI(j) = V_1^4 - 4V_1^2(P_2 Rij + Q_2 Xij) - 4(P_2 Xij - Rij Q_2)^2 \quad (10)$$

For a radial distribution system with "n" number of nodes to be in stable state when

$VSI(j) \geq 0$, for $j = 2, 3 \ldots n$.

The VSI of each bus is computed before and after the installation of shunt capacitors in the modified IEEE 13 bus and 37 bus test systems. Bus number 675, Phase C and bus number 740, phase A is identified as the suitable candidate node in IEEE 13 bus and IEEE 37 bus test systems for placing shunt capacitor which is having lower voltage stability index values.

6. Case Study and Simulation Results

In this work, Radial distribution load flow based on Backward/Forward sweep technique and Harmony Search Algorithms are implemented using MATLAB and tested on modified IEEE 13 bus and 37 node URDN. The original test system is modified [5] by removing the voltage regulator to study the shunt capacitor impacts on bus voltage profiles. The HS algorithm flow chart is illustrated in Figure 8. The pictographic representation of modified IEEE 13 bus and 37 bus URDN is as shown in Figure.9 and Figure 12.

The proposed HSA approach is implemented to identify the optimal shunt capacitor sizing in modified IEEE 13 bus and 37 bus unbalanced Radial distribution systems. The modified IEEE 13 bus-URDN consists of three, two and single phase lines with distributed loads and spot loads. The total active and reactive power loads on the system is 3466 KW and 2102 KVAR. Bus 1 is treated as slack bus and the buses from 2 to13 are modeled as constant PQ buses. 10 MVA, 4.16 kV is taken as base value. The modified IEEE 37 bus URDN has three phase underground cables. The total real power loads on the proposed URDN is 2451.91 KW and reactive power loads is 1217.32 KVAR. The system loads consist of delta connected spot loads with mixture of constant real and reactive power loads, impedance loads and current loads. 30 MVA, 4.8 kV is taken as base values. The substation at bus 1 is considered as the only supply source. The rms values of bus voltages limits are selected as Vmin = 0.9 pu, and Vmax = 1.1pu. 168 U.S. $/KW is taken as real power loss cost per year [2]. The total KVAR injections from shunt capacitors should not go beyond the total KVAR demands of the proposed test systems. A detailed description of the proposed test systems can be found in [5].

To investigate the impact of the shunt capacitors in the proposed test system on the power loss and bus voltage profiles, the following test cases are taken into considered.

Case - I: The bus voltage profiles and total system power losses before capacitor installation.

Case - II: The bus voltage profiles and total system power losses after capacitor installation.

The effective usage of Harmony memory in HSA is based on appropriate parameter values [12]. If the HMCR value selection is too low there will be slow convergence due to selection of very few best harmonies from the HM. If the HMCR value is high (near to1) all the harmonies in the HM are used, the other harmonies are not well explored and this may leads to wrong solution. Therefore the typical HMCR values chosen within 0.7 to 0.95.

The pitch adjustment rate (PAR) based on the bandwidth size is used to generate slightly modified solution in HSA. The pitch adjustment generates a new solution around the existing best solution. A low PAR with narrow bandwidth will limit the exploration only on small subspace in the entire search space and it can lead to slow down the convergence as shown in Figure 2 and Figure 5 for the proposed IEEE 13 bus and 37 bus test systems. Higher PAR with wider BW leads the solution to scatter around some potential optima similar to random search as shown in Figure 3 and Figure 6 for the proposed test systems. Thus the typical PAR value to be selected between 0.1 to 0.5. The randomization component in HSA will increase the solution diversity to find out the global optimum. Test runs were done with various values of PAR and BW and finally chosen HSA parameters towards the optimal solution as shown in Figure 4 and Figure 7 of the proposed optimization problem and the selected HSA parameter values are tabulated in Table 2.

Table 2. Chosen HSA Parameter values

Item	IEEE 13 bus	IEEE 37 bus
HMS size	15	15
HMCR	0.9	0.9
PAR	0.5	0.4
BW	5	5
Total number of iterations	1000	1000

Table 3. IEEE 13 bus voltage profile (magnitude and phase angles)

Bus no	A Phase		B Phase		C Phase	
	magnitude	angle	Magnitude	angle	Magnitude	Angle
650	1	0	1	-120	1	120
632	0.9736	-1	0.9841	-120.6734	0.9605	119.2430
671	0.9522	-2.1490	0.9812	-120.7288	0.9270	118.6696
645	0	0	0.9783	-120.7263	0.9601	119.3061
633	0.9718	-1.0413	0.9830	-120.7021	0.9589	119.2391
692	0.9522	-2.1490	0.9812	-120.7288	0.9270	118.6696
684	0.9520	-2.1615	0	0	0.9259	118.6534
680	0.9522	-2.1490	0.9812	-120.7288	0.9270	118.6696
675	0.9476	-2.2432	0.9819	-120.7790	0.9249	118.7299
652	0.9509	-2.1471	0	0	0	0
646	0	0	0.9771	-120.7368	0.9594	119.3628
634	0.9574	-1.4658	0.9719	-120.9950	0.9475	118.9311
611	0	0	0	0	0.9248	118.6284

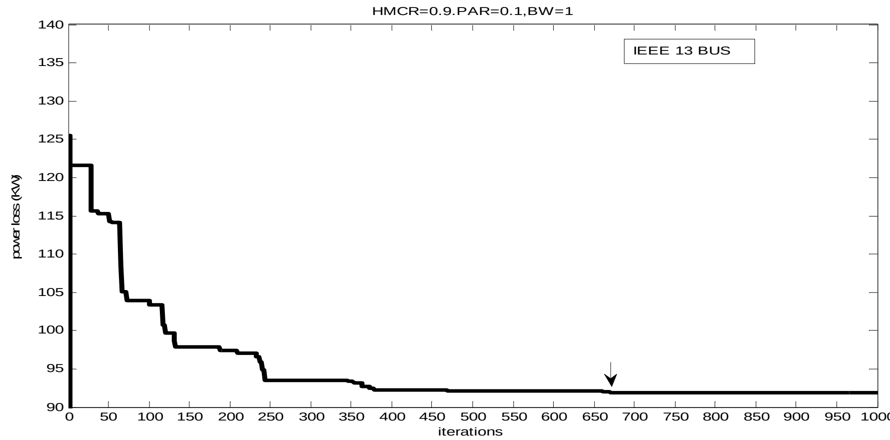

Figure 2. Effect of choosing low values of HSA parameters on convergence of IEEE 13 bus test system solution

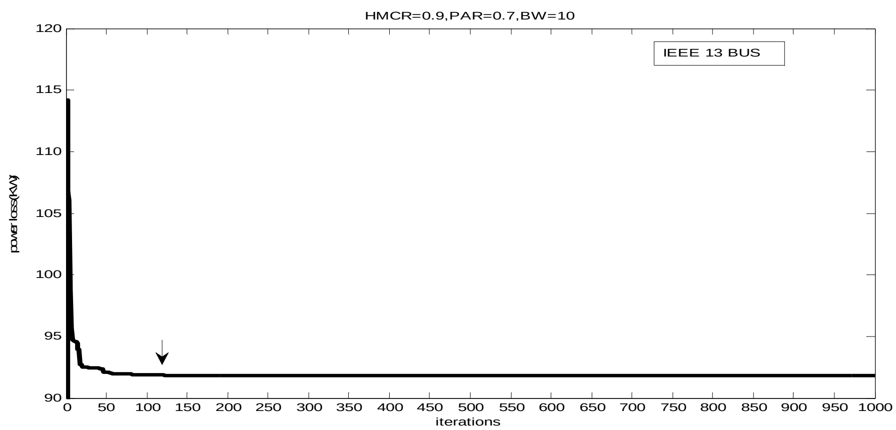

Figure 3. Effect of choosing high values of HSA parameters on convergence of IEEE 13 bus test system solution

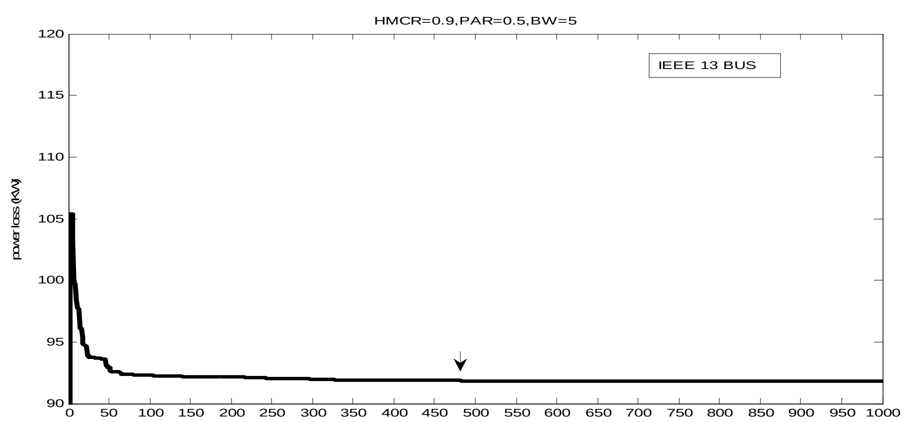

Figure 4. Effect of chosen values of HSA parameters on convergence of IEEE 13 bus test system solution

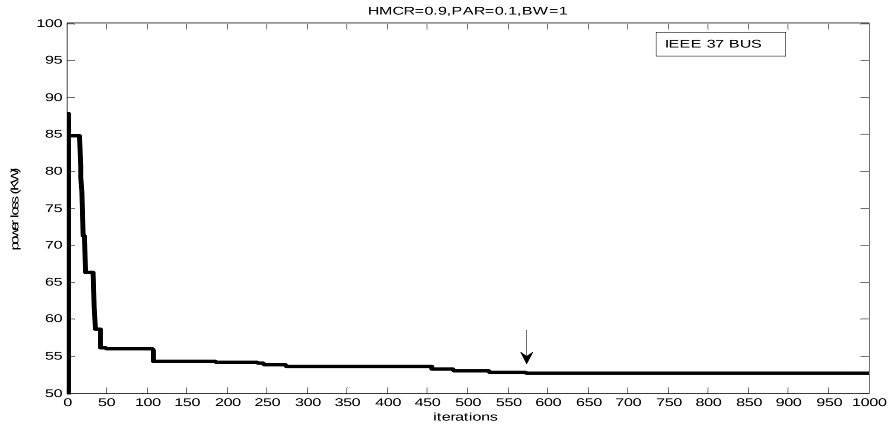

Figure 5. Effect of choosing low values of HSA parameters on convergence of IEEE 37 bus test system solution

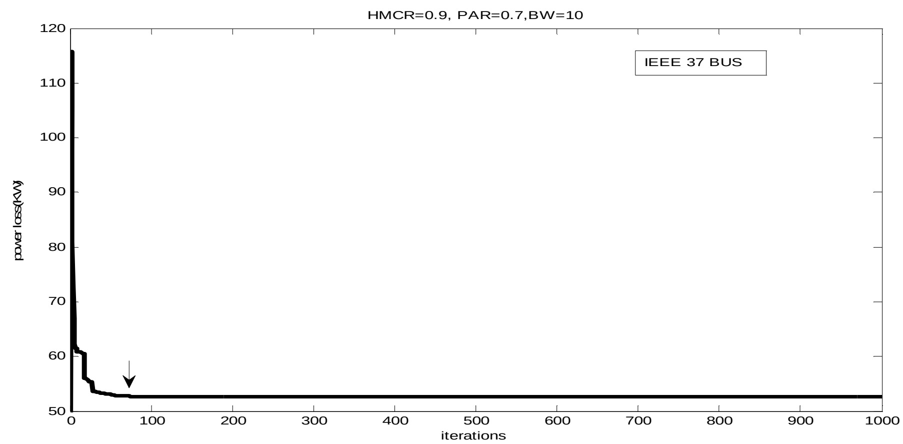

Figure 6. Effect of choosing high values of HSA parameters on convergence of IEEE 37 bus test system Solution

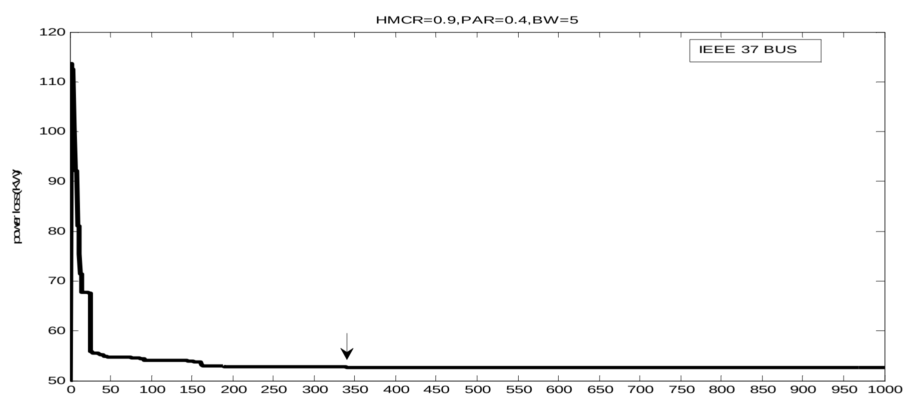

Figure 7. Effect of chosen values of HSA parameters on convergence of IEEE 37 bus test system solution

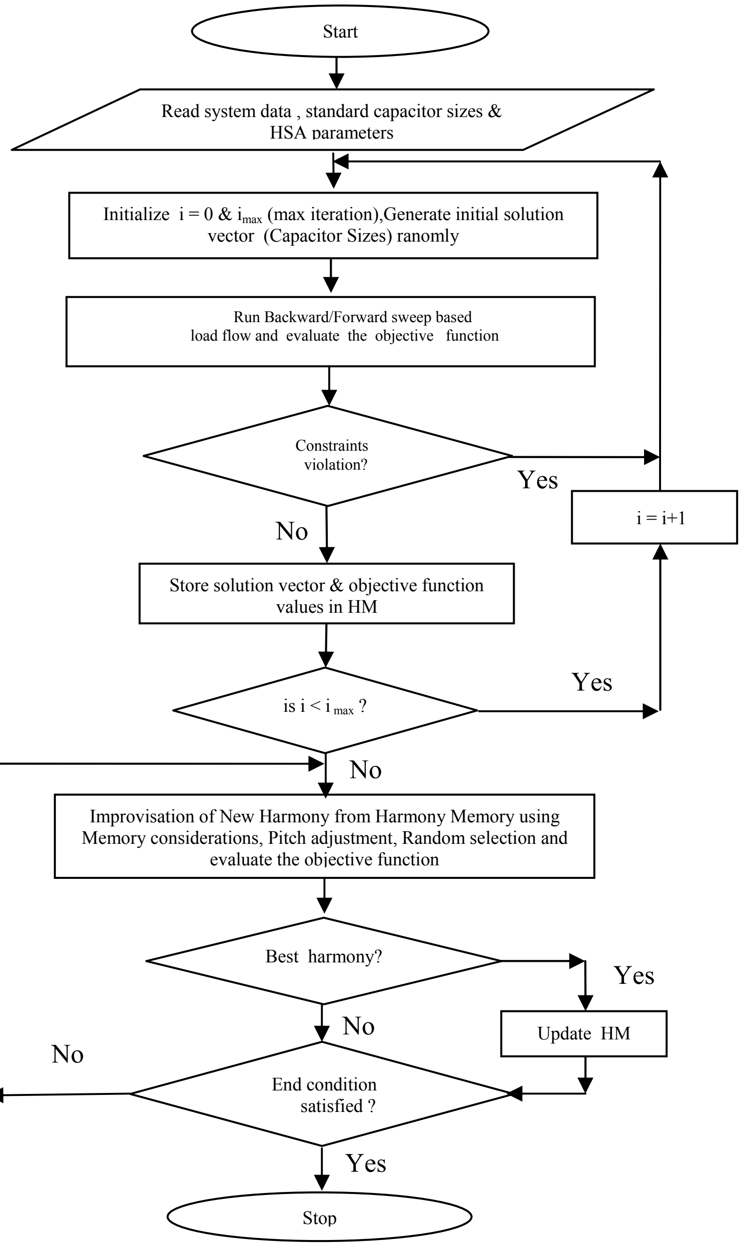

Figure 8. Flow chart of proposed HS algorithm

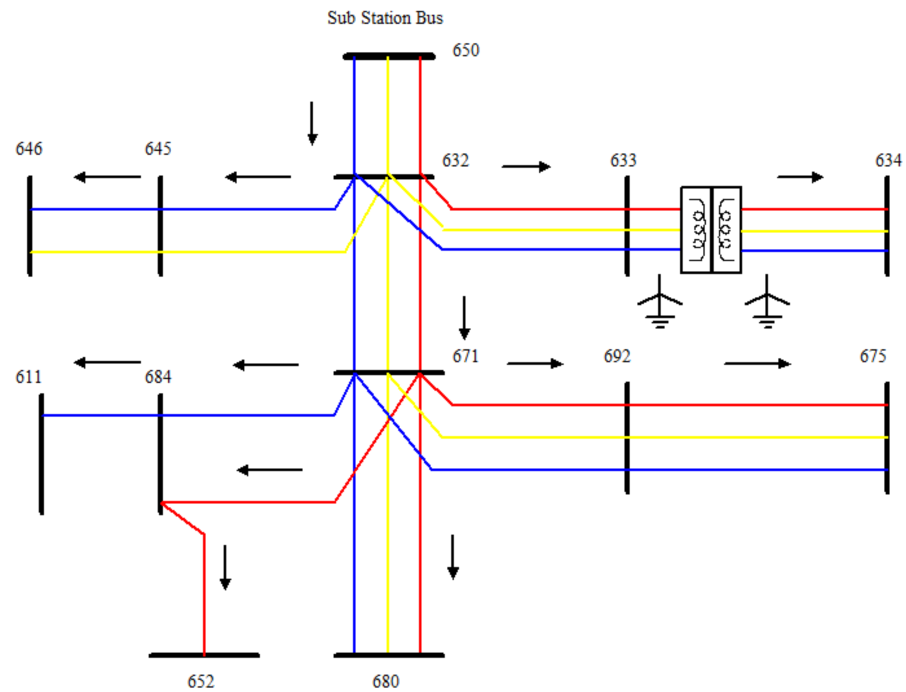

Figure 9. Modified IEEE 13-Bus unbalanced radial distribution network (URDN)

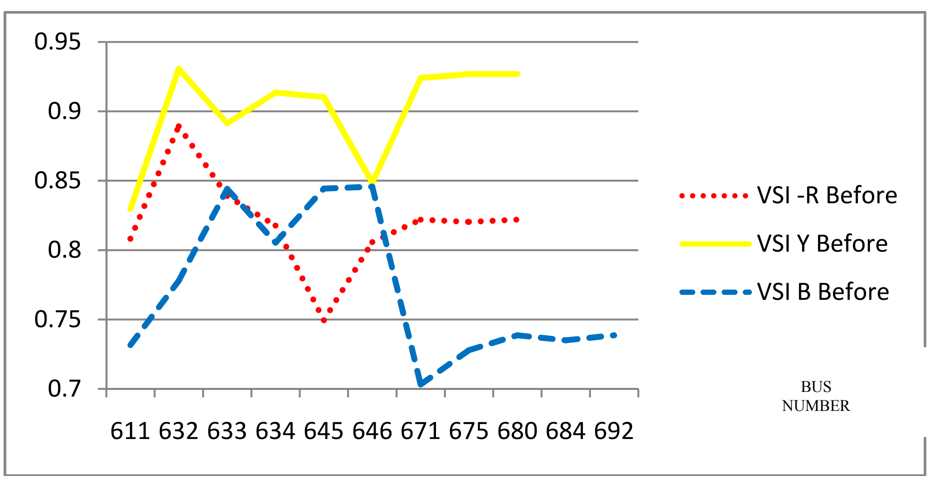

Figure 10. VSI of three phases before capacitor compensation in IEEE 13 bus test system

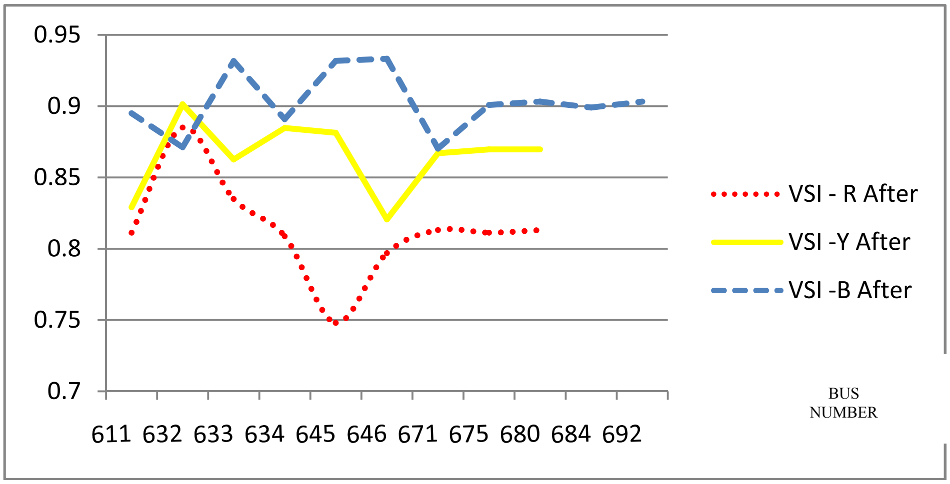

Figure 11. VSI of three phases after capacitor compensation in IEEE 13 bus test system

Table 4. IEEE 13 bus voltage profile (Magnitude and phase angles) after capacitor installation

	A Phase		B Phase		C Phase	
Busno	**Mag**	**Ang**	**Mag**	**Ang**	**Mag**	**Ang**
650	1	0	1	-120	1	120
632	0.9723	-0.3588	0.9756	-121.049	0.9867	118.7852
671	0.9494	-0.8387	0.9642	-121.490	0.9793	117.7681
645	0	0	0.9697	-121.103	0.9863	118.8455
633	0.9705	-0.3997	0.9744	-121.079	0.9851	118.7824
692	0.9494	-0.8387	0.9642	-121.490	0.9793	117.7681
684	0.9492	-0.8519	0	0	0.9782	117.7528
680	0.9494	-0.8387	0.9642	-121.490	0.9793	117.7681
675	0.9464	-0.8833	0.9631	-121.492	0.9801	117.5349
652	0.9481	-0.8374	0	0	0	0
646	0	0	0.9685	-121.113	0.9855	118.9001
634	0.9562	-0.8253	0.9632	-121.377	0.9740	118.4907
611	0	0	0	0	0.9771	117.7292

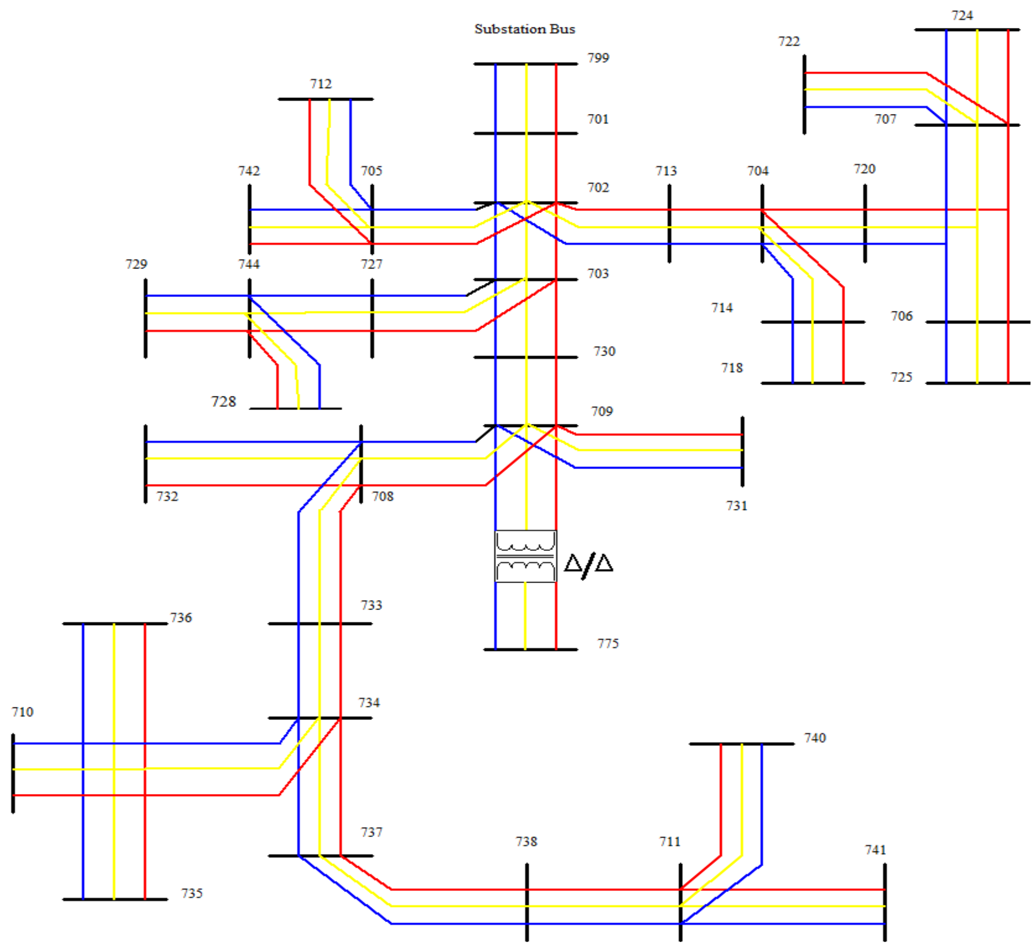

Figure 12. Modified IEEE 37-bus URDN

VSI values before capacitor compensation in each phase of the proposed test systems are shown in Figure 10 and Figure 13. The VSI values after capacitor compensation are shown in Figure 11 and Figure 14. Simulation results reveal that the significant improvements in overall VSI values after reactive power compensation. Voltage profile and angle before placing the shunt capacitors are as shown in Table 3 and Table 5. Voltage profile and angle after placing the capacitor compensation as shown in Table IV and Table 4.

Installation of shunt capacitor of 600 KVAR at phase C of node 675 in modified IEEE 13 bus test system will yield in reduction of power loss from 116.4267 KW to 91.8339 KW and net savings obtained is 3999.59 $/yr. The cost associated with the real power loss is 19559.6856 $/yr prior to the installation of shunt capacitors and the annual cost of real power loss is reduced from 19559.6856 $/Yr to 15560.0952 $/yr after capacitor installation.

Similarly the installation of shunt capacitor of 300 KVAR at phase A of node 740 in modified IEEE 37 bus test system will result in the reduction of power loss from 62.1081 KW to 53.8264 KW and net savings obtained is 1286.32 $/yr. Before the shunt capacitor installation, the cost associated with the real power loss is 10434.1608 $/yr. The annual cost of real power loss is reduced from 10434.1608$/Yr to 9147.8352 $/yr after capacitor installation. Simulation results of proposed test systems are summarized in Table 7. The net savings with the placement of shunt capacitors (in case-II) in the proposed test systems justifies the need for installation of shunt capacitors in appropriate place with optimal rating.

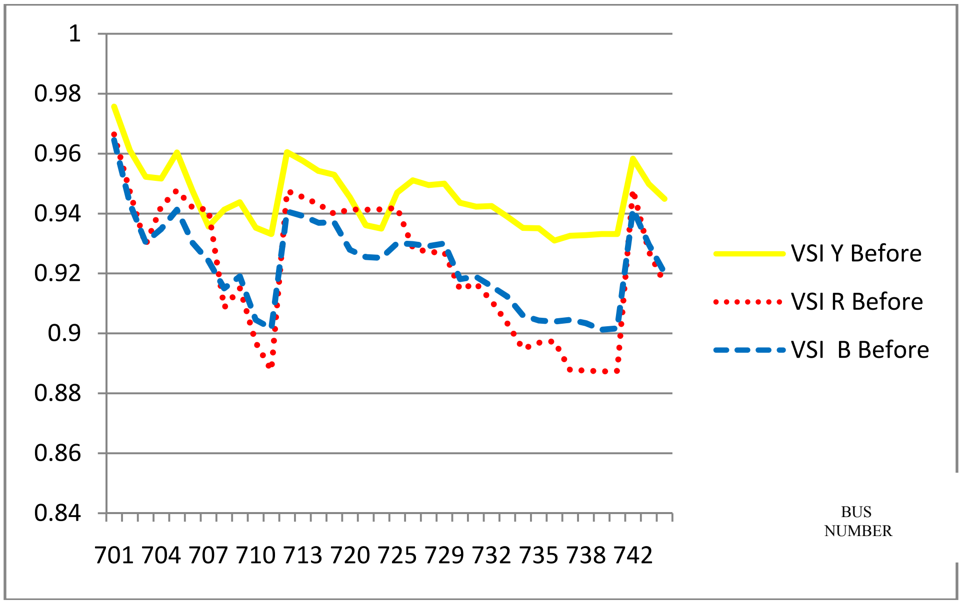

Figure 13. VSI of 3 phases before capacitor compensation IEEE 37 bus test system

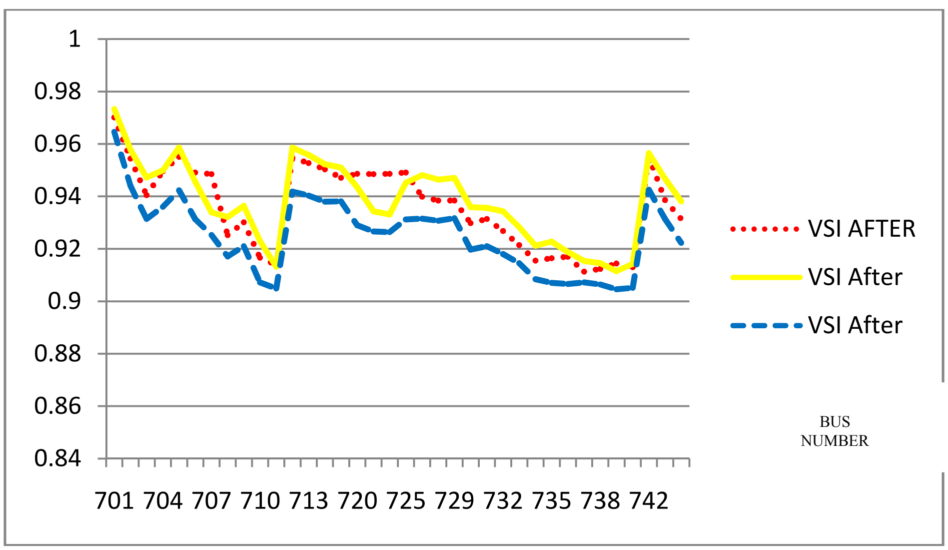

Figure 14. VSI of 3 phases after capacitor compensation in IEEE 37 bus test system

Table 5. Voltage profiles and phase angles of IEEE 37 bus URDN

Voltage profiles and angles Before compensation						
	A Phase		**B Phase**		**C Phase**	
Bus no	**Vmag**	**Angle**	**Vmag**	**Angle**	**V mag**	**Angle**
	(p.u)		**(p.u)**		**(p.u)**	
799	1.0000	0	1.0000	-120	1.0000	120
701	0.9917	0.1933	0.9940	-119.9445	0.9907	120.0036
702	0.9871	0.2799	0.9907	-119.9025	0.9860	119.9975
703	0.9824	0.3391	0.9880	-119.8307	0.9825	119.9598
730	0.9794	0.4329	0.9864	-119.7435	0.9801	119.9699
709	0.9785	0.4573	0.9859	-119.7143	0.9794	119.9743
708	0.9770	0.4955	0.9853	-119.6672	0.9785	119.9704
733	0.9756	0.5278	0.9847	-119.6200	0.9777	119.9673
734	0.9736	0.5864	0.9838	-119.5568	0.9763	119.9634
737	0.9717	0.6169	0.9831	-119.4843	0.9756	119.9526
713	0.9864	0.3107	0.9898	-119.8884	0.9849	120.0285
704	0.9856	0.3364	0.9884	-119.8680	0.9839	120.0761
738	0.9710	0.6375	0.9829	-119.4625	0.9751	119.9479
727	0.9819	0.3609	0.9876	-119.8049	0.9822	119.9741
720	0.9852	0.3786	0.9869	-119.8693	0.9823	120.1454
714	0.9855	0.3374	0.9884	-119.8611	0.9839	120.0782
711	0.9707	0.6598	0.9829	-119.4625	0.9747	119.9449
710	0.9733	0.6249	0.9834	-119.5561	0.9755	119.9890
707	0.9850	0.4004	0.9840	-119.8325	0.9810	120.3134
706	0.9852	0.3795	0.9867	-119.8694	0.9821	120.1560
705	0.9868	0.3098	0.9900	-119.8963	0.9853	120.0335
775	0.9785	0.4573	0.9859	-119.7143	0.9794	119.9743
744	0.9815	0.3655	0.9874	-119.7899	0.9820	119.9772
742	0.9867	0.3111	0.9895	-119.8887	0.9851	120.0598
741	0.9706	0.6671	0.9829	-119.4625	0.9745	119.9441
740	0.9706	0.6743	0.9828	-119.4642	0.9744	119.9465
736	0.9733	0.6268	0.9824	-119.5438	0.9752	120.0418
735	0.9732	0.6394	0.9833	-119.5577	0.9752	119.9906
732	0.9769	0.5071	0.9853	-119.6685	0.9783	119.9720
731	0.9785	0.4590	0.9855	-119.7153	0.9792	119.9946
729	0.9813	0.3671	0.9873	-119.7802	0.9821	119.9779
728	0.9813	0.3742	0.9871	-119.7817	0.9819	119.9871
725	0.9851	0.3799	0.9865	-119.8667	0.9821	120.1679
724	0.9850	0.4015	0.9834	-119.8252	0.9808	120.3448
722	0.9850	0.4031	0.9837	-119.8288	0.9809	120.3304
718	0.9849	0.3423	0.9881	-119.8258	0.9840	120.0809
712	0.9867	0.3267	0.9899	-119.8982	0.9849	120.0354

Table 6. Voltage profiles and phase angles of IEEE 37 bus URDN

Voltage profile and angle After compensation						
	A Phase		**B Phase**		**C Phase**	
Bus no	Vmag	**Angle**	**Vmag**	**Angle**	**V mag**	**Angle**
	(p.u)		**(p.u)**		**(p.u)**	
799	1.000	0	1.0000	-120.	1.0000	120
701	0.9928	0.1337	0.9938	-120.0224	0.9909	120.0008
702	0.9889	0.1769	0.9902	-120.0361	0.9863	119.9956
703	0.9854	0.1761	0.9872	-120.0415	0.9829	119.9591
730	0.9831	0.1990	0.9849	-120.0218	0.9806	119.9724
709	0.9824	0.1996	0.9842	-120.0153	0.9800	119.9779
708	0.9813	0.1998	0.9831	-120.0043	0.9791	119.9758
733	0.9803	0.1940	0.9821	-119.9932	0.9784	119.9744
734	0.9789	0.1857	0.9806	-119.9935	0.9770	119.9736
737	0.9777	0.1398	0.9791	-119.9936	0.9764	119.9663
713	0.9882	0.2076	0.9893	-120.0220	0.9852	120.0266
704	0.9875	0.2332	0.9880	-120.0016	0.9841	120.0743
738	0.9774	0.1126	0.9783	-120.0174	0.9760	119.9637
727	0.9848	0.1978	0.9868	-120.0157	0.9826	119.9733
720	0.9870	0.2753	0.9865	-120.0028	0.9825	120.1437
714	0.9874	0.2342	0.9879	-119.9947	0.9841	120.0764
711	0.9776	0.0871	0.9778	-120.0629	0.9756	119.9630
710	0.9786	0.2238	0.9801	-119.9928	0.9762	119.9991
707	0.9869	0.2971	0.9835	-119.9661	0.9813	120.3118
706	0.9870	0.2762	0.9862	-120.0030	0.9824	120.1544
705	0.9887	0.2067	0.9895	-120.0299	0.9855	120.0316
775	0.9824	0.1996	0.9842	-120.0153	0.9800	119.9779
744	0.9845	0.2024	0.9866	-120.0008	0.9825	119.9765
742	0.9886	0.2080	0.9890	-120.0223	0.9854	120.0580
741	0.9775	0.0943	0.9778	-120.0629	0.9755	119.9621
740	0.9778	0.0551	0.9772	-120.0999	0.9752	119.9704
736	0.9786	0.2257	0.9792	-119.9806	0.9759	120.0519
735	0.9785	0.2382	0.9801	-119.9945	0.9760	120.0007
732	0.9812	0.2113	0.9831	-120.0055	0.9789	119.9774
731	0.9824	0.2014	0.9837	-120.0162	0.9797	119.9983
729	0.9843	0.2040	0.9865	-119.9910	0.9825	119.9772
728	0.9843	0.2111	0.9864	-119.9925	0.9823	119.9864
725	0.9870	0.2766	0.9860	-120.0003	0.9824	120.1663
724	0.9869	0.2982	0.9829	-119.9588	0.9811	120.3431
722	0.9869	0.2998	0.9832	-119.9624	0.9812	120.3288
718	0.9867	0.2392	0.9877	-119.9593	0.9843	120.0791
712	0.9885	0.2236	0.9894	-120.0319	0.9852	120.0335

Table 7. Summary of test results

	IEEE13 bus CASE-I (Before Capacitor Placement)	IEEE 13 bus CASE –II (After capacitor Placement)	IEEE 37 bus CASE-I (Before Capacitor Placement)	IEEE 37 bus CASE –II (After capacitor Placement)
Min value of bus voltage	0.9248	0.9464	0.9706	0.9752
Max value of bus voltage	0.9841	0.9867	0.9940	0.9938
Real Power losses (kW)	116.4267	91.8339	62.1081	53.8264
Reactive power injection (KVAR)	-	Bus 675 Phase C $Q_C = 600$ KVAR	-	Bus 740, Phase A, $Q_C = 300$ KVAR
Cost of total active power loss ($/year)	19559.6856	15560.0952	10434.1608	9147.8352
Loss Reduction (%)	-	20.44	-	12.32
Net Savings (($/year)	-	3999.59	-	1286.32

7. Conclusion

In this proposed work, HSA is utilized to find out the suitable size of shunt capacitor to be placed in the modified IEEE 13 and 37 bus URDN to achieve power loss minimization with improved voltage profile in all nodes. Estimation of voltage stability index of all nodes in the proposed test network is utilized to identify the weakest buses as the candidate nodes for installation of shunt capacitor. The backward / forward sweep based load flow technique is adopted to get faster power flow solutions. From the simulation study, it reveals that the Harmony Search Algorithm is well suited and capable of finding the global or near optimal solution for nonlinear integer optimization problems.

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